

RDA012M4

12 Bit 1.2 GS/s 4:1 MUXDAC

Features

- ◆ 12 Bit Resolution
- ◆ 1.2 GS/s Sampling Rate
- ◆ 4:1 or 2:1 Input Multiplexer
- ◆ Differential Analog Output
- ◆ Input code format: Offset Binary
- ◆ Output Swing: 600 mV with 50 Ω Termination
- ◆ 3.3V NMOS-Compatible Data Inputs
- ◆ Differential ECL or Sinusoidal Clock Input
- ◆ LVDS Compatible Clock Output
- ◆ 10-bit static linearity
- ◆ Reference Output/Input Pin for Accurate Full-Scale Adjustment.
- ◆ 3.3V and -5.2V Power Supply
- ◆ 77 Lead HSD package

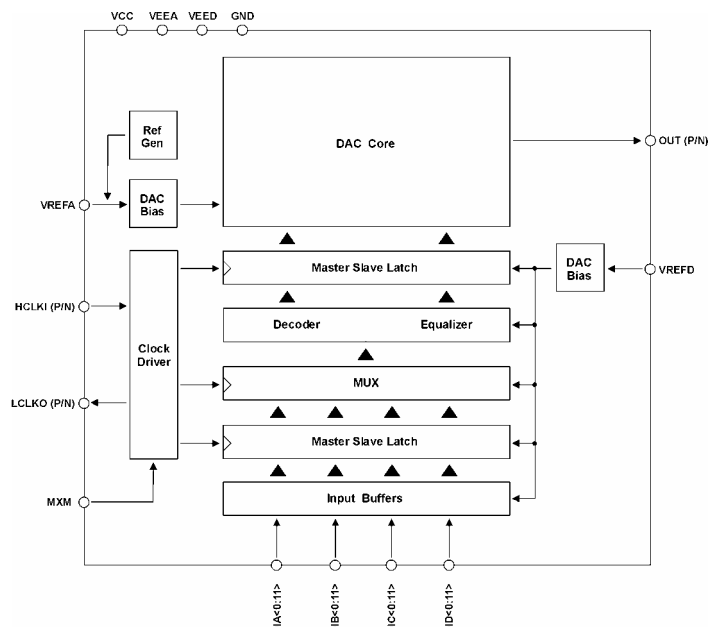


Figure 1 - Functional Block Diagram

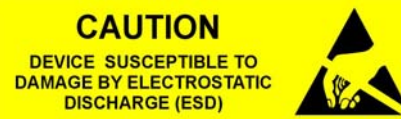
Product Description

The RDA012M4 is a digital-to-analog converter (DAC) with a 4:1 input multiplexer and a maximum update rate of 1.2GS/s. The integrated DAC utilizes a segmented current source to reduce the glitch energy and to achieve high linearity performance. For best dynamic performance, the DAC outputs are

internally terminated with 50Ω resistance, and outputs a nominal full-scale current of 12mA when terminated with external 50Ω resistors. For a convenient interface with most CMOS ICs, the digital data inputs are low voltage NMOS compatible.

Ordering information

PART NUMBER	DESCRIPTION
RDA012M4-HD	12 BIT 1.2GS/s MUXDAC, HSD Package
RDA012M4-DI	12 BIT 1.2GS/s MUXDAC, DIE
EVRDA012M4-HD	RDA012M4-HD Evaluation Board



Absolute Maximum Ratings

Supply Voltages

Between GNDs	-0.3 to +0.3 V
Between VCCs	-0.3 to +0.3 V
VCCs to GND	0 V to +3.8 V

RF Input Voltages

CLKIP, CLKIN to GND	-3 V to 1 V
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HS Digital Input Voltages

DI<0:11>	0 V to VCC
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Output Termination Voltages

OUTP, OUTN to GND	-1 V to 1 V
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Temperature

Case Temperature.....	-40 to +85 °C
Junction Temperature.....	+125 °C
Lead, Soldering (10 Seconds)	+220 °C
Storage.....	-60 to 125 °C

DC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VCC = 3.3V; VEEA = -5.2V; VEED = -5.2V; VREFA = -2V; VREFD = -2V; Clock: 1.2GHz, 0.6Vpp Differential; Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
1.0	DC TRANSFER FUNCTION						
1.1	Differential Nonlinearity	DNL	Maximum of Absolute Value		4		LSB
1.2	Integral Nonlinearity	INL	Maximum of Absolute Value		4		LSB
2.0	TEMPERATURE DRIFT						
2.1	Warm-up Time		After Power-up			30	s
3.0	HIGH CLOCK INPUT (HCLKIP, HCLKIN)						
3.1	Input Resistance	Z _{CIN}	Resistance to VTT	45	50	55	Ω
4.0	DIGITAL INPUTS (DIA<0:11>, DIB<0:11>, DIC<0:11>, DID<0:11>)						
4.1	Input Resistance	R _{DIN}			2K		Ω
5.0	LOW CLOCK OUTPUT (LCLKOP, LCLKON)						
5.1	Common Mode	V _{CM,LCKO}		0.9	1.2	1.5	V
5.2	Amplitude Voltage	V _{CPP,LCKO}	Differential LVDS	250	350	450	mV
6.0	ANALOG OUTPUTS (OUTP, OUTN)						
6.1	Full-scale Output Swing	V _{FSD}	Differential, Terminated Into 50Ω to GND on Each Output	1140	1200	1260	mVpp
6.2	Full-scale Output Swing	V _{FSS}	Single Ended, Terminated Into 50Ω to GND	570	600	630	mVpp
6.3	Full-scale Output Range	V _{FSSRS}	Single Ended, Terminated Into 50Ω to GND (MIN=000h, MAX=FFFh)	-650		0	V
6.4	Output Current	I _{OUT}	Terminated Into 50Ω to GND		12		mA
7.0	ANALOG REFERENCE (VREFA)						
7.1	Reference Voltage	V _{VREFA}	Output from Internal Reference	-1.9	-2	-2.1	V
8.0	DIGITAL REFERENCE (VREFD)						
8.1	Reference Voltage	V _{VREFD}	Output from Internal Reference	-1.9	-2	-2.1	V
9.0	POWER SUPPLY REQUIREMENTS						
9.1	Positive Current	ICC			150		mA
9.2	Negative Current, Analog	IEEA			95		mA
9.3	Negative Current, Digital	IEED			420		mA
9.4	Power Dissipation	P	Total Dissipation		3.3		W
9.5	Power Dissipation	P _{VCC}	Positive Supply		0.5		W
9.6	Power Dissipation	P _{VEEA}	Negative Supply, Analog		0.5		W
9.7	Power Dissipation	P _{VEED}	Negative Supply, Digital		2.3		W

AC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VCC = 3.3V; VEEA = -5.2V; VEED = -5.2V; VREFA = -2V; VREFD = -2V; Clock: 1.2GHz, 0.6Vpp Differential; Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
10.0	DYNAMIC PERFORMANCE						
10.1	SFDR	SFDR 1	F _{CLK} = 800MHz, F _{OUT} = 267MHz		56		dB
10.2	SFDR	SFDR 2	F _{CLK} = 1GHz, F _{OUT} = 333MHz		53		dB
10.3	SFDR	SFDR 3	F _{CLK} = 1.2GHz, F _{OUT} = 400MHz		50		dB
11.0	DATA TIMING (DIA<0:11>, DIB<0:11>, DIC<0:11>, DID<0:11>)						
11.1	Data In to LCLKO Setup	t _{DTLCKST}		300			ps
11.2	Data In to LCLKO Hold	t _{DTLCKHD}		-50			ps

Operating Conditions

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
12.0	HIGH CLOCK INPUTS (HCLKIP, HCLKIN)						
12.1	Amplitude	V _{CPP}	Differential ECL	400	600	800	mV
12.2	Common Mode Voltage	V _{CCM}		-0.8	-1.5	-2	V
12.3	Maximum Frequency	F _{MAX}		1200			MHz
12.4	Minimum Frequency	F _{MIN}				1	MHz
13.0	DIGITAL INPUTS (DIA<0:11>, DIB<0:11>, DIC<0:11>, DID<0:11>)						
13.1	Input High Voltage	V _{IH}		0.9		VCC	V
13.2	Input Low Voltage	V _{IL}		-0.4		0.4	V
14.0	TERMINATION VOLTAGE (VTT)						
14.1	Termination Voltage	V _{TT}	Termination Voltage for HCLKI		-2		V
15.0	ANALOG REFERENCE (VREFA)¹ (note 1)						
15.1	Reference Voltage	V _{REF}		-2.5	-2	-1.2	V
16.0	DIGITAL REFERENCE (VREFD)						
16.1	Reference Voltage	V _{REF}		-2.5	-2	-1.2	V
17.0	POWER SUPPLY REQUIREMENTS						
17.1	Positive Supply Voltage	VCC		3.1	3.3	3.5	V
17.2	Analog Supply Voltage	VEEA		-5.4	-5.2	-5.0	V
17.3	Digital Supply Voltage	VEED		-5.4	-5.2	-5.0	V
18.0	OPERATING TEMPERATURE² (note 2)						
18.1	Case Temperature	T _c	Measured at Bottom Plate	-40		85	°C
18.2	Junction Temperature	T _j				120	°C

¹ The DAC core current is generated from an internal reference that is both temperature and supply dependent. The Internal reference can change up to ±2% by changing the supply voltage within the specified range. It can also change up to ±5% according to operating temperature changes. The change in temperature and supply can be minimized by using a precision external voltage reference source connected to VREFA.

² The part is designed to function with a junction temperature up to 125°C. For the best performance, operation within the specified temperature range with a proper heatsink attached to the device is recommended. The heatsink should be attached to the bottom of the PCB, on a metal pad connect by thermal vias to the metal pad where the part is soldered.

Pin Description and Pin Layout

P/I/O	PIN	NUM.	NAME	FUNCTION
P	7, 16, 39, 62	4	VCC	+3.3V Digital Power Supply
P	1, 68, 71, 72, 73, 74, 75, 76, 77	9	VEEA	-5.2V Analog Power Supply
P	10, 14, 26, 52, 64, 67	6	VEED	-5.2V Digital Power Supply
P	Bottom Plate	-	GND	Ground
I	2	1	VREFA	-2V Reference Voltage
I	12	1	VREFD	Digital Circuitry Bias Reference. Bypass to Ground
I	4	1	VTT	HCLKI Clock Termination Voltage
I	6	1	MXM	Mux Mode Selection: Float – 4:1 (channels A, B, C, D) GND – 2:1 (channels B, C)
I	5	1	HCLKIP	Clock Input
I	3	1	HCLKIN	
I	8	1	LCLKOP	
I	9	1	LCLKON	Low Clock Output
I	11, 13, 15, 17, 18, 19, 20, 21, 22, 23, 24, 25	12	DIA<0:11>	DIA<i> Is Channel A Digital Bit i Input. MSB is bit 11
I	27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38	12	DIB<0:11>	DIB<i> Is Channel B Digital Bit i Input. MSB is bit 11
I	51, 50, 49, 48, 47, 46, 45, 44, 43, 42, 41, 40	12	DIC<0:11>	DIC<i> Is Channel C Digital Bit i Input. MSB is bit 11
I	66, 65, 63, 61, 60, 59, 58, 57, 56, 55, 54, 53	12	DID<0:11>	DID<i> Is Channel D Digital Bit i Input. MSB is bit 11
O	70	1	OUTP	Differential Output
O	69	1	OUTN	

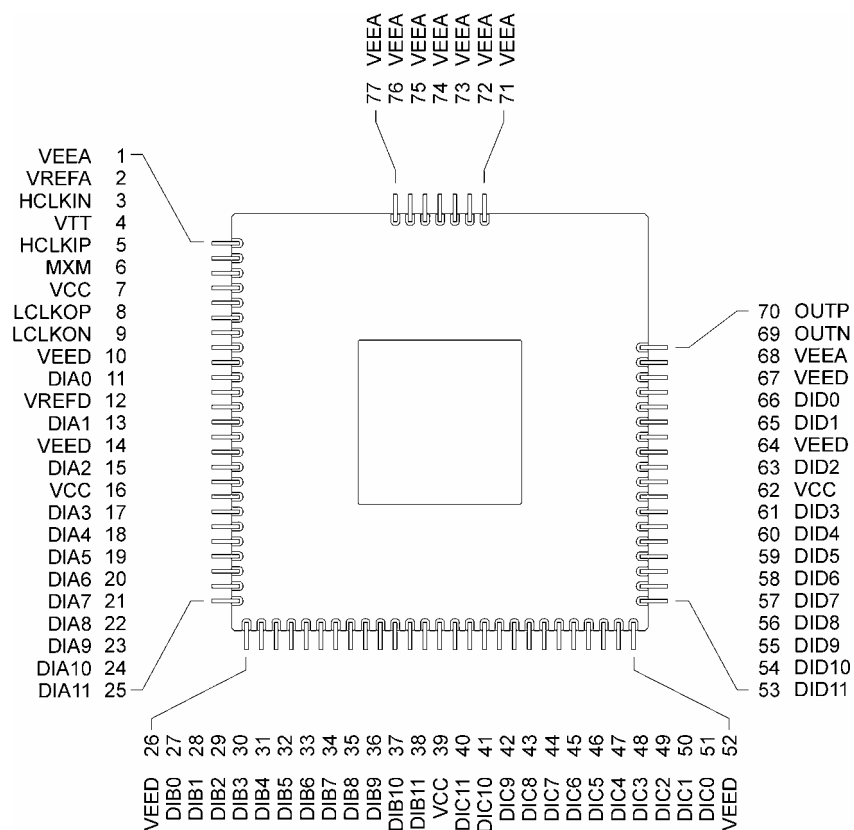


Figure 2 - RDA012M4-HD pinout (top view).

Pad Layout

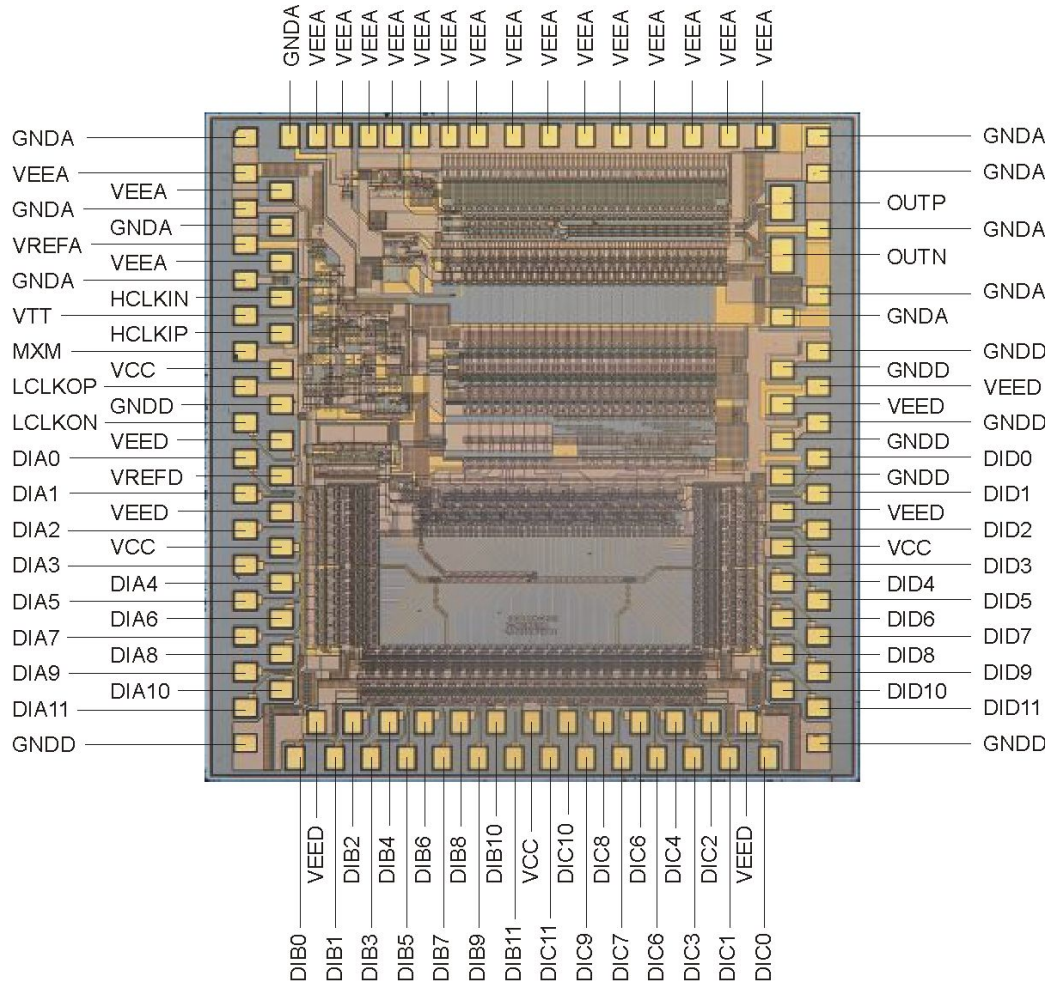


Figure 3 - RDA012M4 pad layout. Photograph for pad layout reference only.

Theory of Operation

For best dynamic and static performance, the DAC employs 4-bit segmentation. The 3.3V NMOS compatible 12-bit digital data inputs are latched by a master-slave flip-flop immediately after the input buffer to reduce the data skew. The four-channel data are combined together by the 48:12 MUX and latched again. The 4 MSB data bits are decoded into thermometer code by a two-stage decoding block, and the 8 LSB data bits are transported through the delay equalizer block. The digital data are synchronized again by a second master slave flip-flop to reduce the switching glitch. The decoded 4 MSB data drive 15 identical current switches, and the 8 LSB data drive 8 current switches. The output nodes from the LSB current switches are connected to the analog output through an R-2R ladder to generate the binary output.

The DAC output full-scale voltage follows the relationship $V_{FS} = 0.3xV_{REF}$. An internal reference circuit with approximately -10dB

supply rejection is integrated on chip for application convenience. The reference pin is provided for monitoring and for bypass purposes. To band-limit the noise on the reference voltage, the reference pin should be bypassed to the GNDA node with capacitance > 100pF. The VREF pin can also be used to override the internal reference with an accurate, temperature-compensated external voltage reference.

The timing diagram is shown in Figure 4. The 1.2GHz external clock (HCLKI) is divided by 2 and 4 resulting in the MUX internal selection signals S0 and S1. A low-speed clock (LCLKO) is provided to drive the external digital. The four-channel data input are latched with an internal clock that is synchronized with the LCLKO. Controlled by S0 and S1, input data are fed to the 1.2GS/s DAC in the order shown.

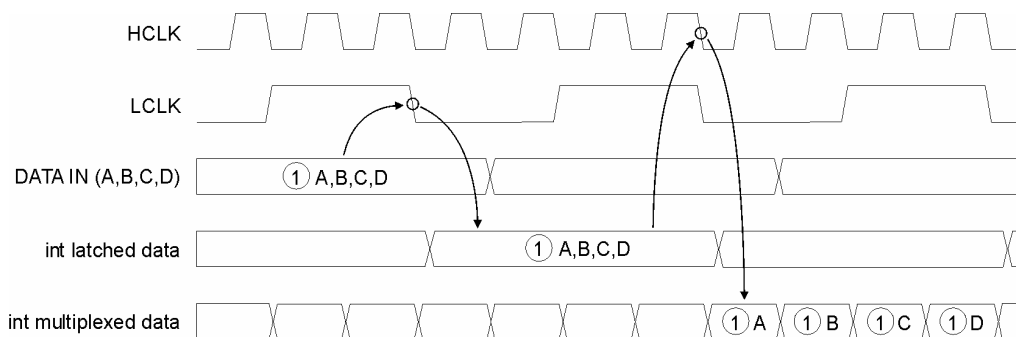


Figure 4 - Input Timing Diagram.

Signal Description

HIGH SPEED INPUT CLOCK.

The RDA012M4 high-speed clock input is differential and can be driven from typical ECL circuits. Also a differential sinusoidal clock can be used. The HCLKIP and HCLKIN inputs, are internally terminated with $50\ \Omega$ to VTT which should be connected to a well decoupled -2.0 volt supply. Since the MUXDAC's output phase noise is directly related to the input clock noise and jitter, a low-jitter clock source is ideal. The internal clock driver generates very little added jitter (~ 100 fs). A 500MHz MUXDAC output demands a white noise induced clock jitter of less than 250fs for a 10-bit equivalent, 62dB SNDR.

DATA INPUT.

The data inputs are 3.3V NMOS-compatible. The data is interleaved according to significant bit. For example, consecutive data pins will occur as DIA0, DIB0, DIC0, DID0, DIA1, DIB1, etc.

OUTPUT CLOCK.

Output clock LCLKOP and LCLKON are supplied for the DSP/FPGA/ASIC. They are LVDS compliant and needs to be terminated with a 100Ω resistor in front of the receiving buffer or the receiving pins of the ASIC/DSP.

For application convenience, the data input's setup and hold time is specified with respect to the LCLKO. It should be noted that LCLKOP and LCLKON are driven by the MUXDAC and the waveforms of these signals are better defined at the receiver end; that is, near the ASIC/DSP chip that provides the input data for the MUXDAC. The system designer should consider the delay associated with the signal routing in the system's timing budget.

The setup and hold time of the LCLK to data transition are defined at the MUXDAC side. Data transitions of the data input have to occur during the "Valid Data Transition Window." The timing margin seen from the MUXDAC is $T_P - T_S$ where T_P is the LCLKO period and T_S is the setup time, assuming that the ASIC chip takes LCLKO as the clock input and its outputs are latched at the

falling edge of the clock. From the ASIC/DSP end, however, the timing margin is decreased by the amount equal to the sum of the data delay and clock delay between the two chips.

ANALOG OUTPUT.

The outputs OUTP and OUTN should both be connected though a $50\ \Omega$ resistor to ground. This will give a full-scale amplitude of 0.6 volt (both outputs must be terminated), 1.2 volt differentially. The output common mode can be changed by terminating the load resistors to a different voltage. However, the device is optimized to perform best when connected to a voltage between 0 and 1 volt. For reliable operation, the output termination voltage should not exceed 3 volts.

REFERENCE.

VREFA is provided for added control of the full-scale amplitude output. The internal reference circuit is designed to provide -2.0 volts, which can change up to $\pm 5\%$ as the supply voltage and/or operating temperature changes. If the user prefers accurately control the output full-scale signal, an external voltage reference with low output impedance to override the internal reference should be used. The output full-scale voltage follows the relationship $V_{FS} = 0.3 \times V_{REF}$. Note that the MUXDAC is optimized to have the best performance with a reference voltage of -2.0 volts. The output resistance of the reference node is $560\ \Omega \pm 10\%$. VREFD allows adjusting of the digital circuitry bias point for varying input voltage swings. In most cases, VREFD should be bypassed to GND.

Typical Operating Circuit

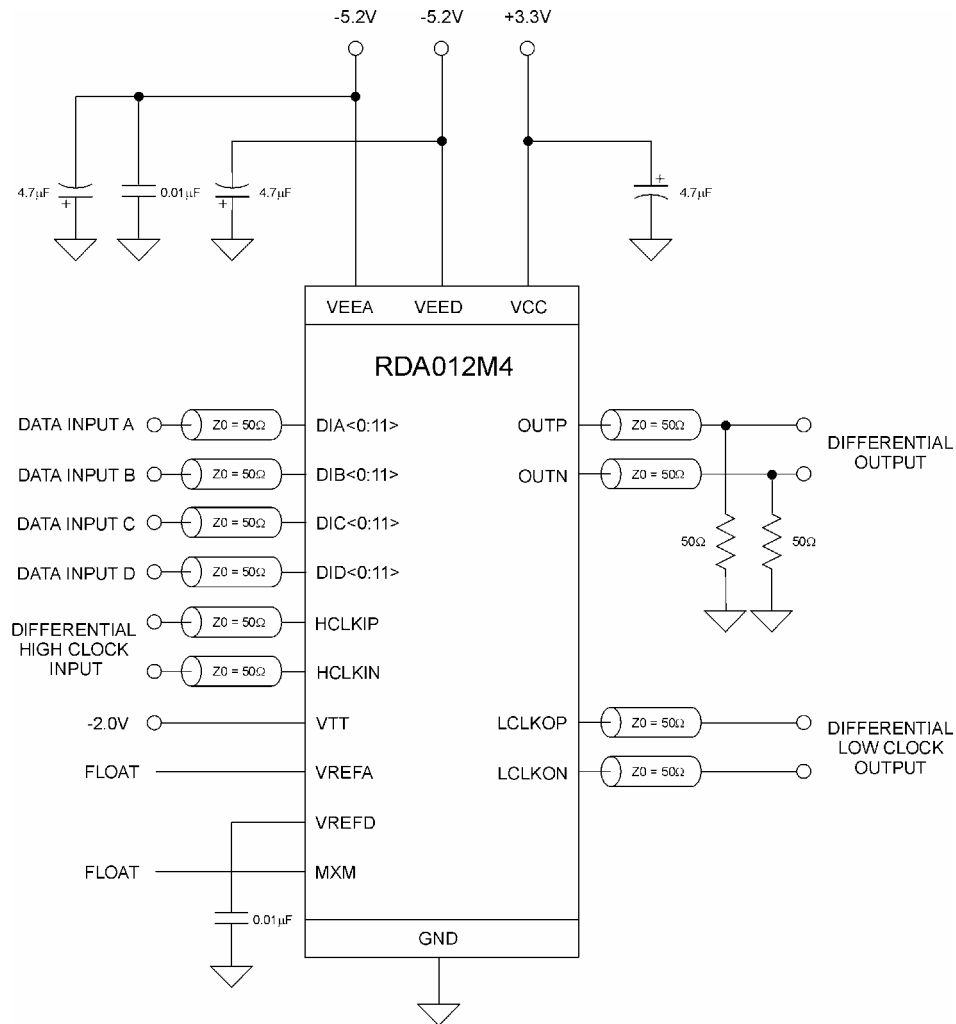


Figure 5 - RDA012M4 typical operating circuit using the internal voltage reference.

Typical Performance

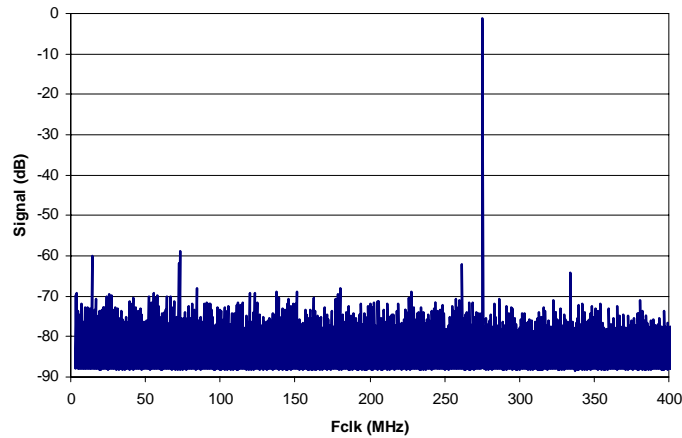


Figure 6 – Output spectrum at Fclk=800MHz, Fout=270MHz

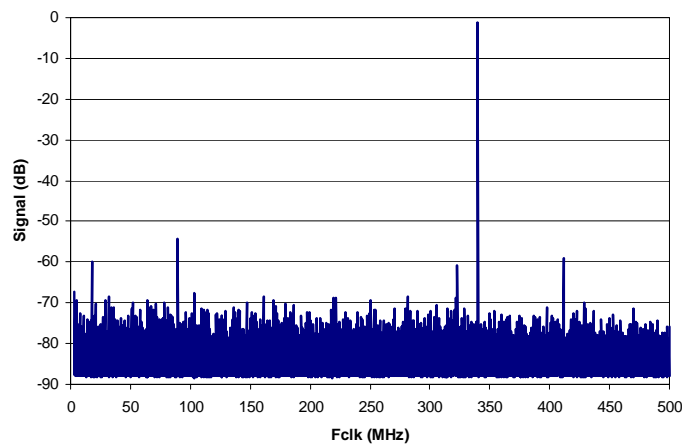


Figure 7 - Output spectrum at Fclk=1000MHz, Fout=340MHz

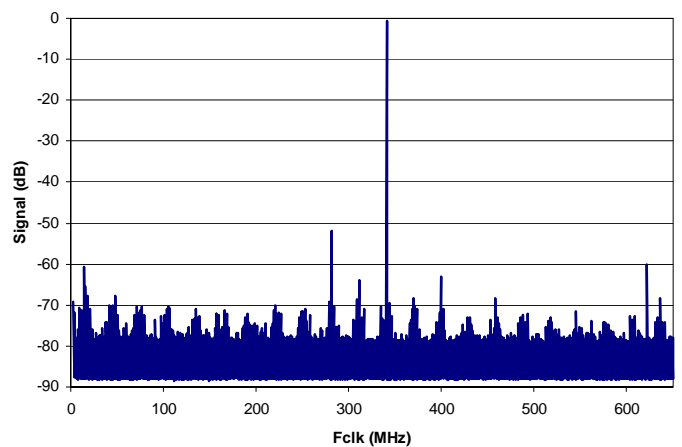


Figure 8 - Output spectrum at Fclk=1200MHz, Fout=340MHz

Package Information

The package is a 77 pin HSD with a heat sink slug on the package's bottom. The leads are gull-winged

formed and trimmed to 0.053 inch (1.35 mm) in length.

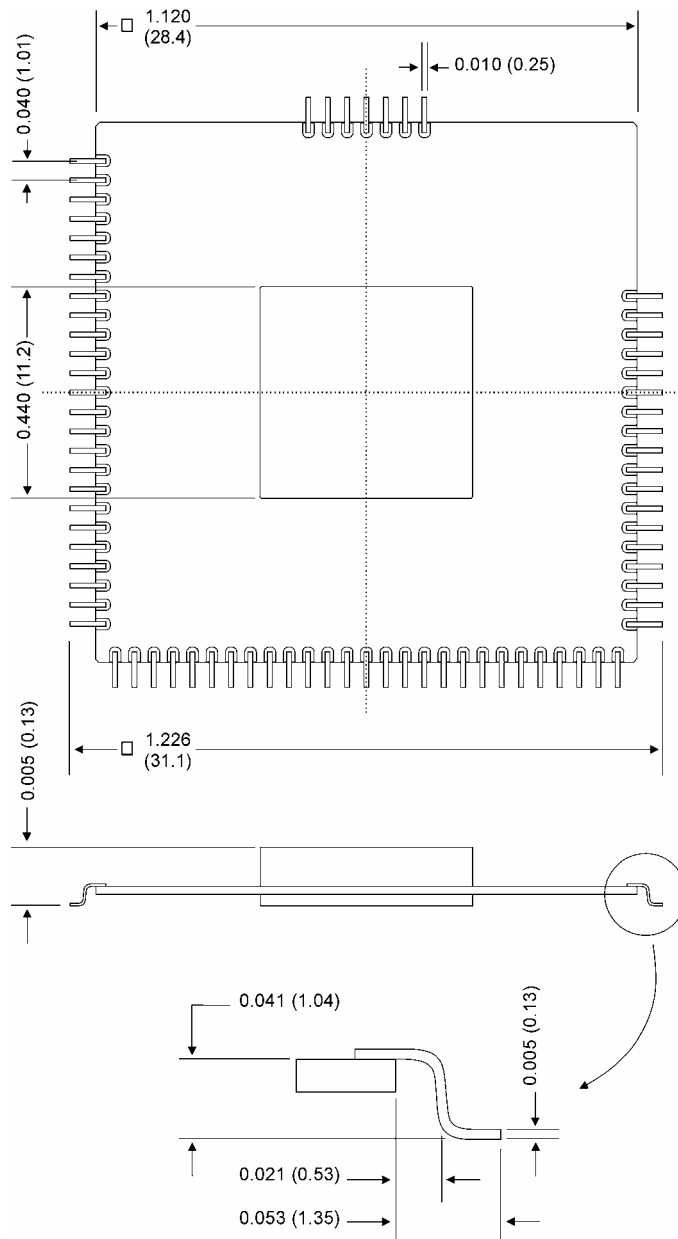


Figure 9 - RDA012M4-HD package, dimensions shown in inches (mm).

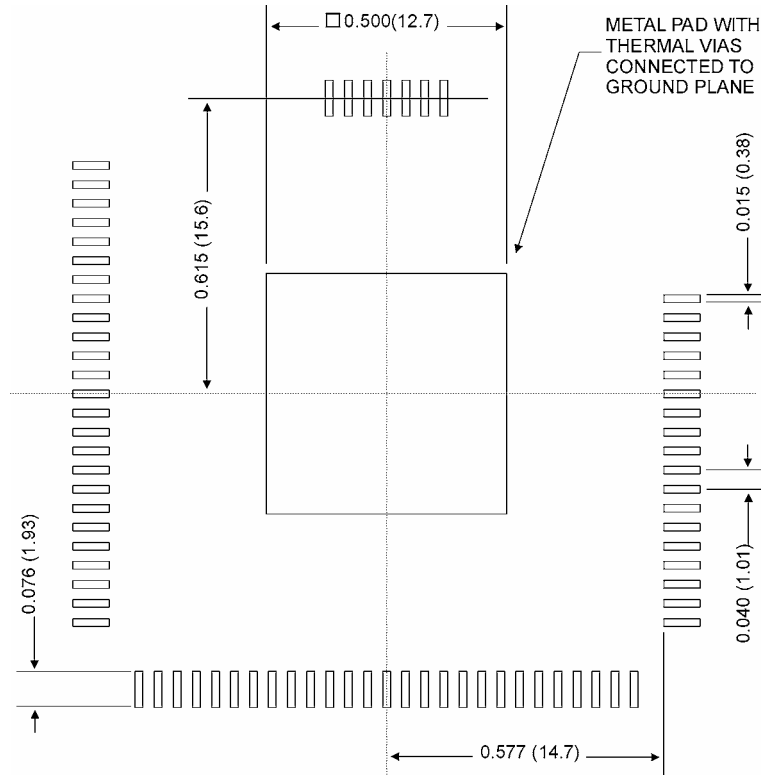


Figure 10 - RDA012M4-HD footprint, dimensions shown in inches (mm).