

RDX004M4

10 Bit 4 GHz 1:4 Demultiplexer

Features

- ◆ 10 Bit Differential Input
- ◆ 4 GHz Operating Frequency
- ◆ Selectable 1:4, 1:2, 1:1 Mode
- ◆ Staggered or Simultaneous Output
- ◆ Grey to Binary Converter
- ◆ Selectable DDR clock
- ◆ Reset for multiple device synchronization
- ◆ Pseudo Random Pattern Generator
- ◆ LVDS Compatible Output
- ◆ Latency of 3 to 9 Clocks Depending on Operating Mode
- ◆ 6 W Power Dissipation
- ◆ BGA package
- ◆ Companion Chip for RAD004

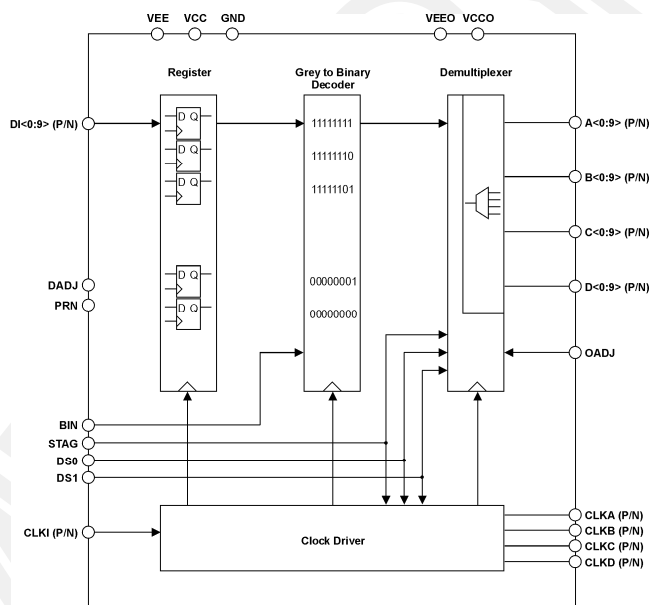


Figure 1 - Functional Block Diagram

Product Description

The RDX004M4 was developed as an output demultiplexer for the Teledyne Scientific family of analog to digital converters. Four control signals are used to select features and device operation mode. BIN enables the grey to binary converter. DS0 and DS1 select the demultiplexer mode. It can operate in 1:4, 1:2, and direct mode 1:1. When in demultiplexer

mode STAG selects the staggered or simultaneous output. Although the RDX004M4 was developed as a companion chip for the Teledyne Scientific analog to digital converters, it can also be used as a generic demultiplexer. For this application the grey to binary converter can be disabled reducing the power dissipation.

Ordering information

PART NUMBER	DESCRIPTION
RDX004M4-DI	10 Bit 4 GHz 4:1 DEMUX DIE
RDX004M4-BG	10 Bit 4 GHz 4:1 DEMUX, BGA Package
EVRDX004M4-BG	RDX004M4 Evaluation Board

CAUTION
DEVICE SUSCEPTIBLE TO
DAMAGE BY ELECTROSTATIC
DISCHARGE (ESD)



Absolute Maximum Ratings

Supply Voltages

Between GNDs	-0.3 to +0.3 V
Between VEEs	-0.3 to +0.3 V
VCCs to GND	-1 V to +6 V

RF Input Voltages

DI<0:9>P, DI<0:9>N to GND	-1 to +1 V
CLKIP, CLKIN to GND	-1 to +1 V

DC Analog Input Voltages

DADJ to GND.....	VEE to +1 V
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DC Digital Input Voltages

DS0, DS1 to GND	-6 to +1 V
BIN to GND	-6 to +1 V
STAG to GND	-6 to +1 V
PRN to GND	-6 to +1 V

Output Termination Voltages

A<0:9>P, A<0:9>N to GND	-2.5 to +3 V
B<0:9>P, B<0:9>N to GND	-2.5 to +3 V
C<0:9>P, C<0:9>N to GND	-2.5 to +3 V
D<0:9>P, D<0:9>N to GND	-2.5 to +3 V
CLKAP, CLKAN to GND	-2.5 to +3 V
CLKBP, CLKBN to GND	-2.5 to +3 V
CLKCP, CLKCN to GND	-2.5 to +3 V
CLKDP, CLKDN to GND	-2.5 to +3 V

Temperature

Case Temperature.....	-15 to +85 °C
Junction Temperature.....	+125 °C
Lead, Soldering (10 Seconds)	+220 °C
Storage.....	-40 to 125 °C

Electrical Specification

PARAMETER	SYMBOL	CONDITIONS, NOTES	TEST LEVEL	MIN	TYP	MAX	UNITS
CLOCK INPUT (CLKI(P/N))							
Clock Input Differential Voltage	VDIF _{CLKI}	Differential		200	600	1000	mV
Clock Input Common Mode	VCM _{CLKI}	Differential		-1.45		0.5	V
Clock Input Resistance	R _{CLK}				50		Ω
CLOCK OUTPUT (CLKA(P/N), CLKB(P/N), CLKC(P/N), CLKD(P/N))							
Clock Output Common Mode	VCM _{CLKO}	Differential			0		V
Clock Output Differential Voltage	VDIF _{CLKO}	Differential			800		mV
DATA INPUT (DI<0:9>(P/N))							
Data Input Differential Voltage	VDIF _{DATAI}	Differential		200	600	1000	mV
Data Input Common Mode	VCM _{DATAI}	Differential		-1.45		0.5	V
Data Input Resistance	R _{DATAI}				50		Ω
Data Input Capacitance	C _{DATAI}						pF
DIGITAL INPUT (BIN, STAG, PRN, DS[1:0])							
Digital Input Voltage	V _{DIGI}			VEE-1.0		GND+1.0	V
Digital Input Resistance	R _{DIGI}				10K		Ω
Digital Input Capacitance	C _{DIGI}					0.5	pF
DATA OUTPUT (A<0:9>(P/N), B<0:9>(P/N), C<0:9>(P/N), D<0:9>(P/N))							
Data Output Common Mode	VCM _{DATAO}	Differential (Adjustable by VCCO)			0		V
Data Output Differential Voltage	VDIF _{DATAO}	Differential			800		mV
TIMING CHARACTERISTICS							
Clock Input							
Frequency	F _{CLK}					4	GHz
Cycle Period	T _{CLK}			250			ps
Clock Pulse High	t _{CLKHI}				125	150	ps
Clock Pulse Low	t _{CLKLO}				125	150	ps
Clock Output							
Clock to Data Output Skew	t _{SKCKDT}	Per channel (CLKA to A, CLKB to B, CLKC to C, CLKD to D)					ps
Data Input							
DI<0:9> to CLKI Setup	t _{STDTCK}				10		ps
DI<0:9> to CLKI Hold	t _{HDDTCK}				40		ps
Data Output							
Propagation (HL) from CLKI	t _{HLCKDT}				110		ps
Propagation (LH) from CLKI	t _{LHCKDT}				110		ps
REFERENCE							
DADJ							
Input Voltage	V _{DADJ}			V _{EE}	-1.0	0	V
Input Resistance	R _{DADJ}				150		Ω
OADJ							
Input Voltage	V _{OADJ}			V _{EE}	-1.0	0	V
Input Resistance	V _{OADJ}				150		Ω
POWER SUPPLY							
Positive Supply	V _{CC}			4.75	5.0	5.25	V
Negative Supply	V _{EE}			-5.45	-5.2	-4.95	V
Positive Output Supply	V _{CCO}						V
Negative Output Supply	V _{EEO}						V
Positive Current Supply	I _{CC}						mA
Negative Current Supply	I _{EE}						mA
Power Dissipation	P _D				6		W
OPERATING TEMPERATURE							
Junction Temperature	T _J			-40		125	°C
Ambient Temperature	T _A			-40		85	°C

Pin Description

P/I/O	PIN	NUM.	NAME	FUNCTION
P	F15, H15, L15, P15	4	VEE	VEE Power Supply
P	E15, J15, K15, N15	4	VCC	VCC Power Supply
P	D8, D10, D12, D14, F4, G4, H4, L4, N4, P4, R7, R9, R11, R14	14	VEEO	VEE Power Supply for Output Buffers
P	D2, D7, D9, D11, E4, K4, M4, R4, R6, R10, R13	11	VCCO	VCC Power Supply for Output Buffers
P	A1, A2, A3, A4, A5, A14, A15, A16, A17, A18, B1, B2, B3, B4, B15, B18, C1, C2, C3, C4, C15, C18, D5, D6, D13, D15, D16, D17, D18, E2, E3, E16, E17, E18, F18, G15, J4, K3, L3, M15, N18, P2, P16, P17, P18, R2, R5, R8, R12, R15, R18, T1, T18, U1, U2, U3, U4, U5, U12, U15, U17, U18, V1, V2, V3, V4, V9, V14, V15, V16, V17, V18	72	GND	Ground
I	C16	1	DADJ	Digital Level Adjustment (range from 0V to -2V)
I	B16	1	OADJ	Output Level Adjustment (range from 0V to -2V)
I	N17, N16, M18, L16, K18, J17, J16, H18, G16, G17	10	DI<0:9>P	DI<i>P / DI<i>N Is Differential Digital Bit i Input. MSB is Bit 9.
I	M17, M16, L18, K16, J18, H17, H16, G18, F16, F17	10	DI<0:9>N	
I	L17	1	CLKIP	CLKIP / CLKIN Is Differential Input Clock
I	K17	1	CLKIN	
I	T17	1	DS0	Multiplexer Mode Select: DS1 DS0 Mode 0 0 1:2 0 1 1:1 1 0 RESERVED 1 1 1:4
I	R17	1	DS1	
I	U16	1	BIN	Grey to Binary Decoding Enable: Active high (ground)
I	T16	1	STAG	Staggered Mode Select: Active high (ground)
I	R16	1	PRN	Pseudo random pattern generator: Active high (ground)
I	B17	1	DDR	DDR clock mode
I	C17	1	RST	RESET
O	V12, T8, T6, P1, K1, F1, C6, B8, C12, C14	10	A<0:9>P	A<i>P / A<i>N Is Differential Digital Bit i of Channel A Output. MSB is bit 9.
O	V13, T9, T7, R1, L1, G1, C5, B7, C11, C13	10	A<0:9>N	
O	B12	1	CLKAP	CLKAP / CLKAN Is Differential Channel A Clock
O	B11	1	CLKAN	
O	T12, U8, V5, P3, K2, H3, D1, C8, B10, A13	10	B<0:9>P	B<i>P / B<i>N Is Differential Digital Bit i of Channel B Output. MSB is bit 9.
O	T13, U9, V6, R3, L2, J3, E1, C7, B9, A12	10	B<0:9>N	
O	F3	1	CLKBP	CLKBP / CLKBN Is Differential Channel B Clock
O	G3	1	CLKBN	
O	U13, V10, U6, T2, M2, H2, D4, A7, A9, B14	10	C<0:9>P	C<i>P / C<i>N Is Differential Digital Bit i of Channel C Output. MSB is bit 9.
O	U14, V11, U7, T3, N2, J2, D3, A6, A8, B13	10	C<0:9>N	
O	M3	1	CLKCP	CLKCP / CLKCN Is Differential Channel C Clock
O	N3	1	CLKCN	
O	T14, T10, V7, T4, M1, H1, F2, B6, C10, A11	10	D<0:9>P	D<i>P / D<i>N Is Differential Digital Bit i of Channel D Output. MSB is bit 9.
O	T15, T11, V8, T5, N1, J1, G2, B5, C9, A10	10	D<0:9>N	
O	U10	1	CLKDP	CLKDP / CLKDN Is Differential Channel D Clock
O	U11	1	CLKDN	

Pin Layout (TOP view)

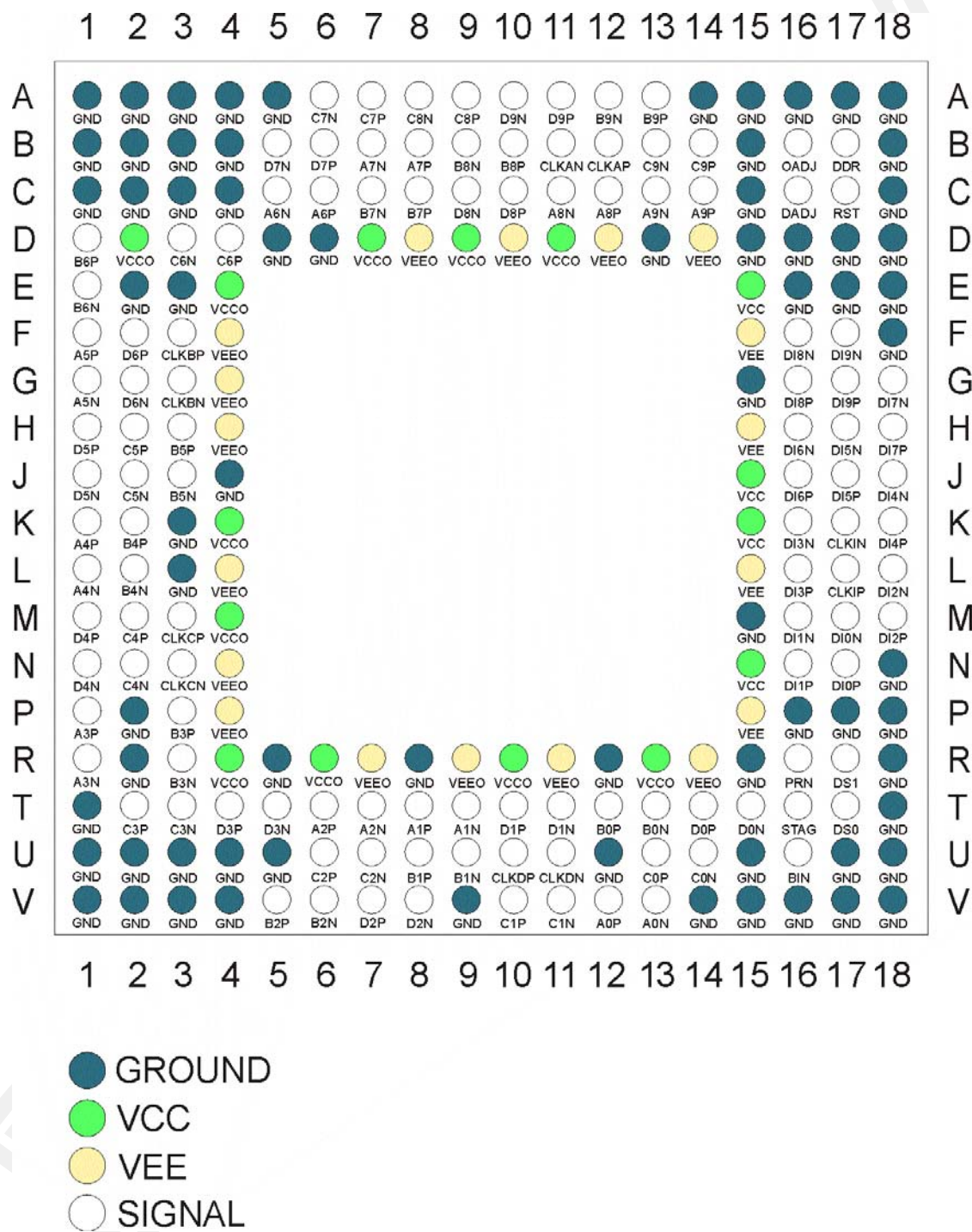


Figure 2 - RDX004M4-BG pinout (top view).

Package Information

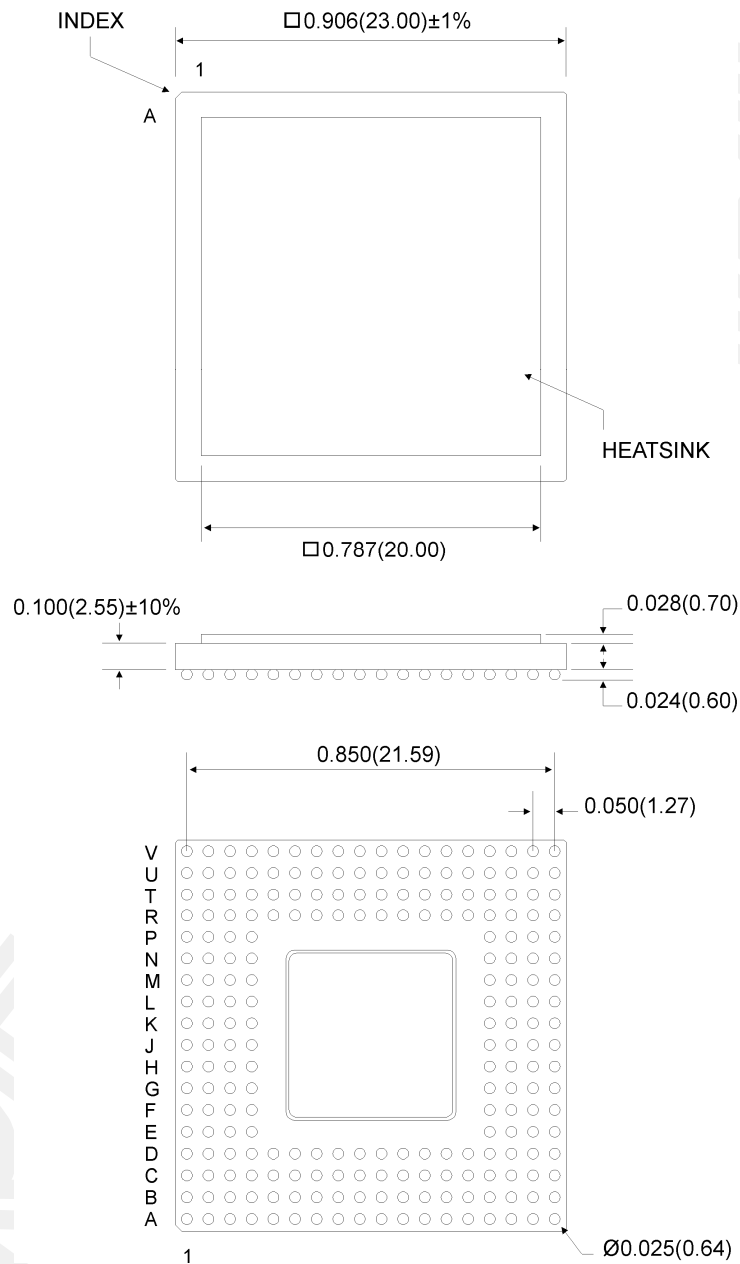


Figure 3 - RDX004M4-BG package, dimensions shown in inches (mm).