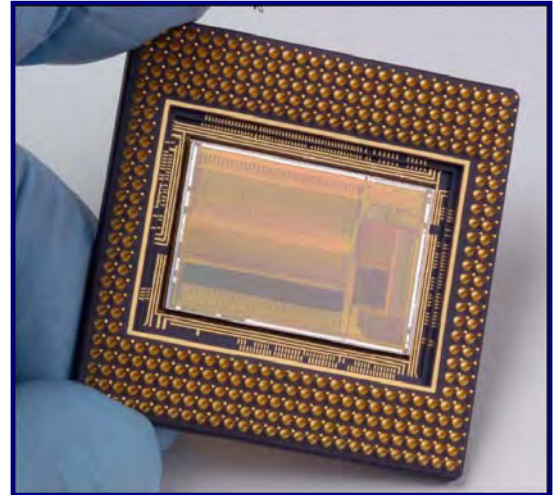


Teledyne Imaging Sensors SIDECAR™ ASIC Development Kit & Focal Plane Electronics

The **SIDECAR™ ASIC** is designed to manage all aspects of imaging array operation and output digitization.

The **SIDECAR™ ASIC** provides:

- 36 input channels, including channels for reference output, window output and temperature sensor.
- Up to 500 kHz A/D conversion with 16-bit resolution per channel.
- Up to 10 MHz A/D conversion with 12-bit resolution per channel.
- Preamp gain: 0dB – 27dB in 3dB steps.
- 32 programmable digital I/O signals (clock generation).
- 20 programmable bias voltages/currents.
- 16-bit fully programmable microcontroller.
- Efficient power-down modes.
- 1-24 digital input/output channels for data transfer (LVDS or CMOS).
- < 150 mW at 100 kHz 32-channel 16-bit A/D operation.
- Requires one power supply, one fixed reference and one master clock for operation.



The **SIDECAR™ ASIC** has been designed as a compact focal plane electronics on a single chip for Teledyne Imaging Sensor's **HAWAII-1RG™** and **HAWAII-2RG™** focal plane arrays supporting all possible modes of operation. The **SIDECAR™ ASIC** also supports the 16-megapixel **HAWAII-4RG-10** as well as the future 16-megapixel **HAWAII-4RG-15** and 64-megapixel **HAWAII-8RG-10** focal plane arrays, where -10 and -15 denote the pixel pitch in microns. The **SIDECAR™ ASIC** is also being used as a control and data acquisition system for general imaging applications including those utilizing CCDs.

The **SIDECAR™ ASIC** development kit represents a powerful, low-cost, highly flexible, small footprint, and low-power solution for ground-based applications and well as the development platform for airborne and space-based applications. TIS offers proven assembly code for several standard readout modes and provides support for custom applications and optimizations based on customer needs.

The **SIDECAR™ ASIC** assembly code included in the development kit supports the following modes:

- Full-field, 32 output, slow readout (up to 500 kHz) mode
- Correlated double sampling, Fowler sampling, and up-the-ramp sampling
- Window operation (including multiple windows)

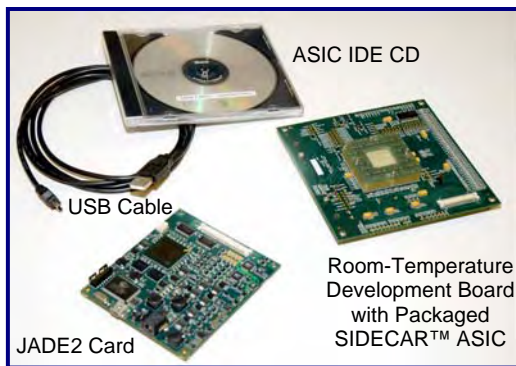
Custom **SIDECAR™ ASIC** assembly code can readily be developed to support

- Guide mode operation
- Different integration and sub-row integration times
- Fast mode readout (up to 10 MHz)
- Selectable outputs (1, 4 or 32)
- As well as other operational modes for the **HAWAII-RG** family of focal plane arrays.

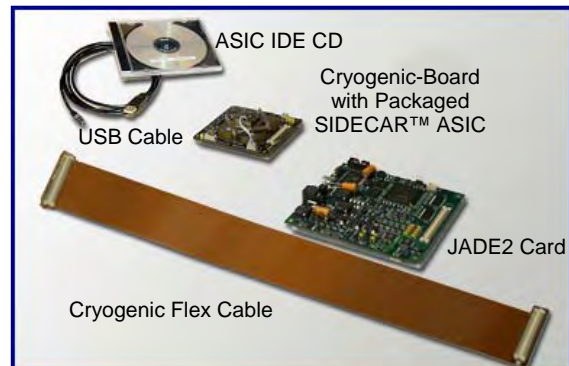
SIDECAR™ ASIC kit standard and upgrade¹ configurations:

The SIDECAR™ ASIC kit is offered as Room-Temperature (RT) Development kit and Cryogenic Focal Plane Electronics (FPE) kit. The RT kit is a lab/demo system designed for flexibility and testability; it is not optimized for performance. The cryogenic FPE kit on the other hand, is designed as the focal plane electronics for the HAWAII-RG family of focal plane arrays and is optimized for performance. Both, the RT Development kit and the Cryogenic FPE kit represent complete solutions, i.e. all hardware and software needed to run a focal plane array is provided. The table below shows the kit configurations and upgrade options offered by Teledyne Imaging Sensors:

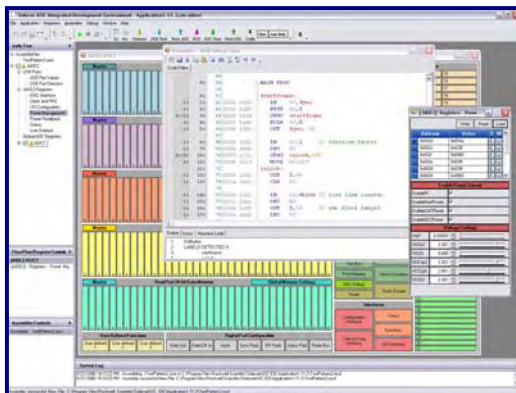
CONFIGURATION	A	B	C	D ¹	E ¹	ASIC Only
SIDECAR™ ASIC Packaged in a 337-pin LGA Ceramic Package	X	X	X	X	X	X
SIDECAR™ ASIC Room Temperature Development/Evaluation Board	X	-	X	-	-	-
SIDECAR™ ASIC Cryogenic Board	-	X	X	X	X	-
SIDECAR™ ASIC Cryogenic Flex Cable to connect SIDECAR™ ASIC Cryogenic Board to JADE2 Card	-	X	X	X	-	-
JADE2 Card for Interface between the SIDECAR™ ASIC and PC	X	X	X	-	-	-
Mini USB 2.0 Cable to connect the JADE2 Card to a PC	X	X	X	-	-	-
CD containing the SIDECAR™ ASIC IDE (Integrated Development Environment), Software, Assembly Code and Documentation	X	X	X	X	X	-



Contents of the RT Development Kit (Temp: 10 to 50 °C)



Contents of the ASIC Cryogenic FPE Kit (Temp: 32 to 300 K)



Integrated Development Environment (IDE)

Acronyms:

- **SIDECAR**: System for Image Digitization Enhancement Control And Retrieval
- **ASIC**: Application Specific Integrated Circuit
- **HAWAII-xRG**: HgCdTe Astronomy Wide Area Infrared Imager with xK by xK pixel, Reference pixel, and Guide mode; x = 1, 2, 4, 6, and 8
- **LVDS**: Low-Voltage Differential Signaling
- **CMOS**: Complementary Metal-Oxide-Semiconductor
- **CCD**: Charge Coupled Device
- **JADE**: JWST ASIC Drive Electronics
- **IDE**: Integrated Development Environment
- **FPE**: Focal Plane Electronics

For more information, please email **Richard Blank** at rblank@teledyne.com or call **(805) 373-4083**.