EVRDA012M4MS

12 Bit 1.3 GS/s 4:1 MUXDAC-MS Evaluation Board

Features

- Option of 2 mating connector board for input: UHD or SMA
- On-Board Balun Conveniently Converts High-Speed Clock Input to Differential Clock
- Master-slave mode for dual synchronous operation
- Fully Assembled and Tested MUXDACMS for your evaluation and prototyping needs

Product Description

The EVRDA012M4MS is an evaluation board designed to demonstrate the performance of the RDA012M4MS, a 1.3GS/s, multiplexing digital-to-analog converter IC. The multiplexed input feature eases the requirement for the data interface and the master-slave operation allows synchronized operation. The evaluation kit consists of two assembled printed circuit boards: one hosting the MUXDAC IC, and one the input connection.

There are two different input boards available, allowing the user to select SMA or UHD connectors.

A third option is to use the Teledyne Scientifics' programmable data generator (RGA012M4) to supply the data. The data generator board allows the user to evaluate the MUXDACMS without any data generating equipment. Only a sampling clock input is required.

For added convenience, the input high speed clock is converted on board into a differential clock using a high-frequency balun.

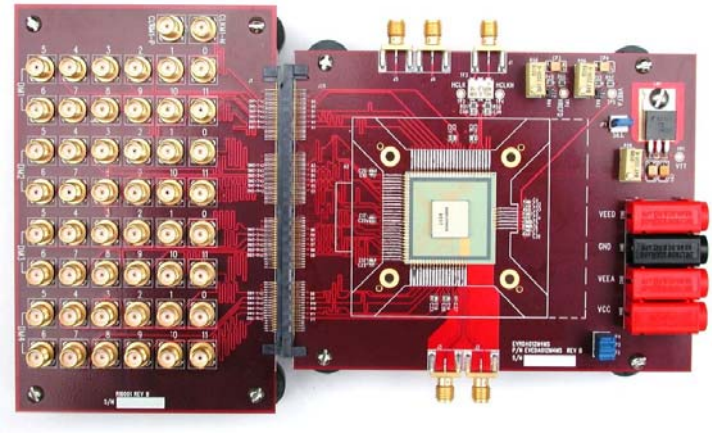

Figure 1 – EVRDA012M4MS-HD-SMA

Ordering information

PART NUMBER	DESCRIPTION
EVRDA012M4MS-HD-SMA	RDA012M4MS-HD Evaluation Board w/ SMA Input Connection Board
EVRDA012M4MS-HD-UHD	RDA012M4MS-HD Evaluation Board w/ UHD Input Connection Board

Signal Description

Power Supplies

The evaluation board requires both a negative and positive supply voltage, and separate digital and analog supplies. VEEA is the analog –5.2V supply, VEED is the digital –5.2V supply. VCC is a +3.3V supply needed for the digital interface.
Connect the power supplies to the evaluation board using banana cables. There is no need for power-up sequencing.

Inputs

The EVRDA012M4MS has three mating options for input. For connector based data input, the user may choose the SMA connector mating board, or UHD (Ultra High Density from Gore) mating board. The third option is the Teledyne Scientifics' RGA012M4, a programmable FPGA-based data generator board. This board allows users to program their own data vectors for the MUXDACMS to sample. All that must be provided is the external sampling clock for the EVRDA012M4MS. See the RGA012M4 user guide for more information.
The EVRDA012M4MS data input is NMOS (3.3V) compatible with Bit(11) being the input most significant bit (MSB) and Bit(0) the least significant bit (LSB).
The termination on data input lines are grounded through JP2, JP3, and JP4. By not having the termination directly connected to ground allows the use of different data input standards, like HSTL-I which have a termination voltage of 0.75V.
The MUXDACMS operates on 4:1 multiplexing mode only. The jumper JP1 controls the SEL (mode SELection) signal, which selects the master-slave operating mode. Leave JP1 uncapped for master mode or jump it for slave mode.
The sampling input clock signal is supplied through an SMA connector, J1, and is converted into a differential signal through a high frequency balun. The differential clock can be checked at TP3 and TP4. The other input clock, LCLKI, is used for synchronization when in slave mode. It should be connected to LCLKO of the master MUXDACMS.
VREFA and VREFD are –2V references that are derived from the power supplies and made available to the MUXDAC. Potentiometer R56 and R50 in this circuit may have to be adjusted to achieve the nominal –2V. Test points are provided for probing purposes. It is a good idea to check that VREFA and VREFD are nominally –2V after power up to achieve optimum performance from the MUXDAC. Likewise, potentiometer R58 may need adjustment to ensure a VTT value of –1.3V, the termination voltage for the differential sampling clock.

Outputs

The analog output (OUTP, OUTN) of the MUXDAC is available on the SMA connectors J2 and J3. OUTP and OUTN should be terminated with 50Ω impedance to ground.
The data clock (LCLKOP, LCLKON) is LVDS compatible and its frequency is HCLK divided by 4. It should be terminated with differential 100Ω impedance at the receiving side. When operating in a master-slave configuration, it is used for synchronization by the slave MUXDACMS.

PC Board Layout

The EVRDA012M4 is fabricated using six layers of FR4 material. Interface to the input board is through the QSE-080-01-F-D-EM2 high-speed edge connector from Samtec.

All data and clock signals are treated as 50Ω transmission lines. Figure 2 is the layer stack of the evaluation board, including layer thickness.

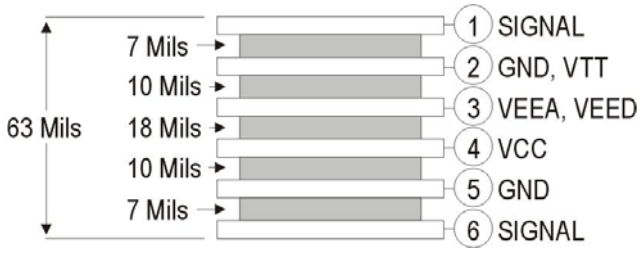

Figure 2 - EVRDA012M4MS layer stack

Components

Table 1: Jumper and Test Point List

DESIGNATOR / SIGNAL	SETTINGS	FUNCTION
JP1 / SEL (Master-Slave-Select)	OFF: SEL is HIGH (internal) ON: Link SEL to GND	OFF: Master mode ON: Slave mode
JP2, JP3, JP4 / DTERM	ON: connect data termination to ground	Set data termination voltage
TP1 / VTT	Nominally –1.3V	Test point
TP2 / VREFD	Between -1.8V and -2.2V	Test point
TP3 / HCLKP	HCLKP = positive sample clock	Test point
TP4 / HCLKN	HCLKN = negative sample clock	Test point
TP5 / VREFA	Between –1.8V and –2.2V	Test point

Table 2: Component List

DESIGNATOR	QTY	DESCRIPTION
C1-C7, C10-C12, C14, C16-C19, C41	16	22pF Capacitors (0603 size)
C20-C23, C26-C29, C31-C37, C40	16	0.1uF Capacitors (0603 size)
C38, C39, C45	3	0.1uF Capacitors (0805 size)
CP1	1	22uF Capacitor (3528 size)
CP2, CP3, CP4	3	4.7uF Capacitors (3528 size)
R1-R48	48	50Ω Resistor (0402 size)
R49, R55	2	120KΩ Resistor (0805 size)
R50, R56	2	200KΩ Potentiometer (64YPOT)
R51, R52	2	10KΩ Resistor (0805 size)
R53, R54	2	RESERVED (0805 size)
R57, R60	2	250Ω Resistor (0805 size)
R58	1	50Ω Potentiometer (64YPOT)
R59	1	1250Ω Resistor (0805 size)
TF2	1	Balun (ADTL2-18)
J20	1	Edge Connector (QSE-080-01-F-D-EM2)
J1, J2, J3, J4, J5	3	SMA Connector (142-0701-851)
BN1, BN2, BN3, BN4	4	Banana Plug Sockets
JP1	1	2 Pin Header
JU1, JU2	2	3 Pin Header
LM1	1	Adjustable Regulator (LM337)
RA1, RA2	2	Shunt Regulator (TLV431ASNT1)
H2	1	MUXDACMS (RDA012M4MS)

Board Configuration

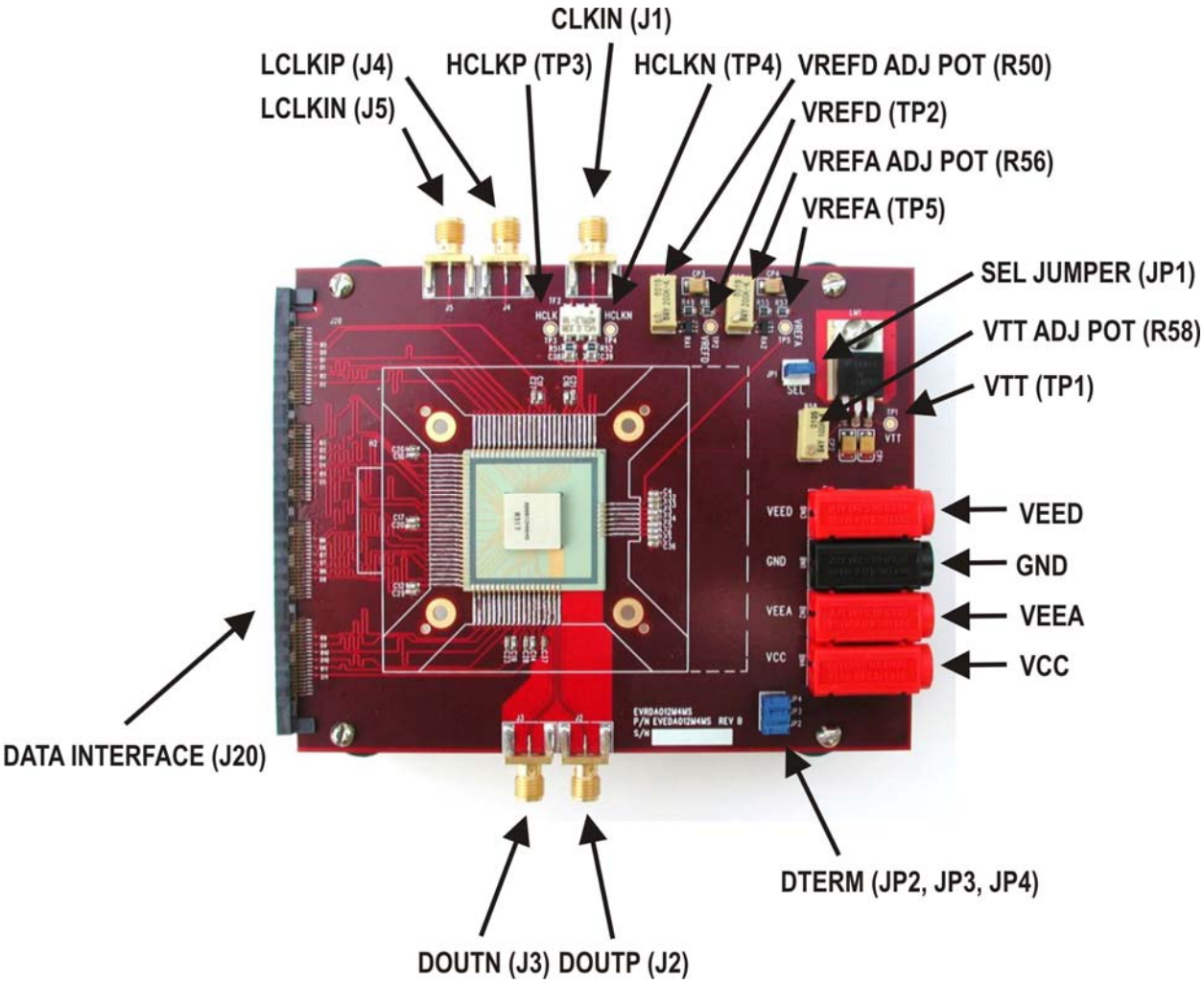

Figure 3 - EVRDA012M4MS board configuration

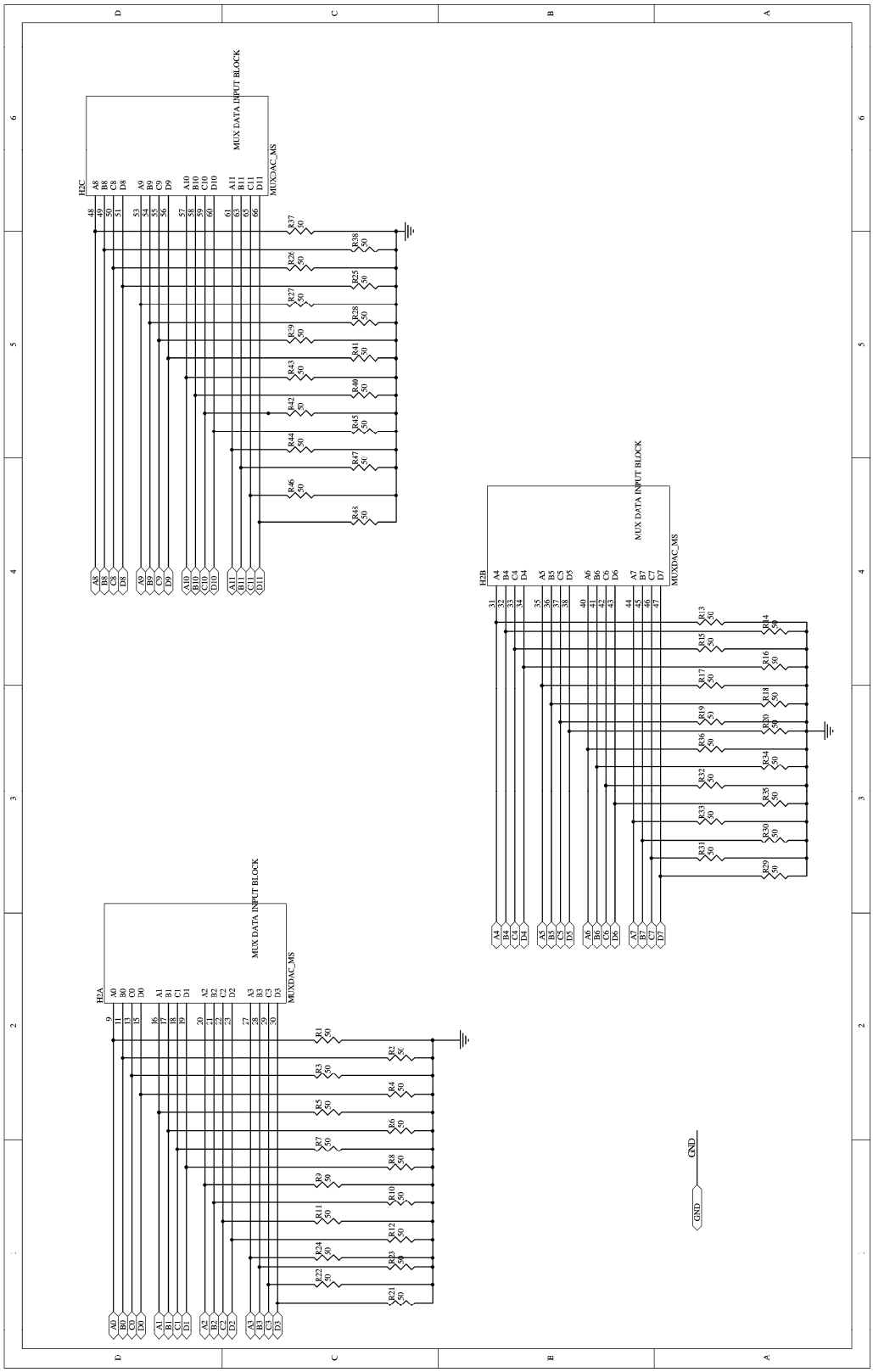

Figure 4 - EVRDA012M4MS schematics (1)

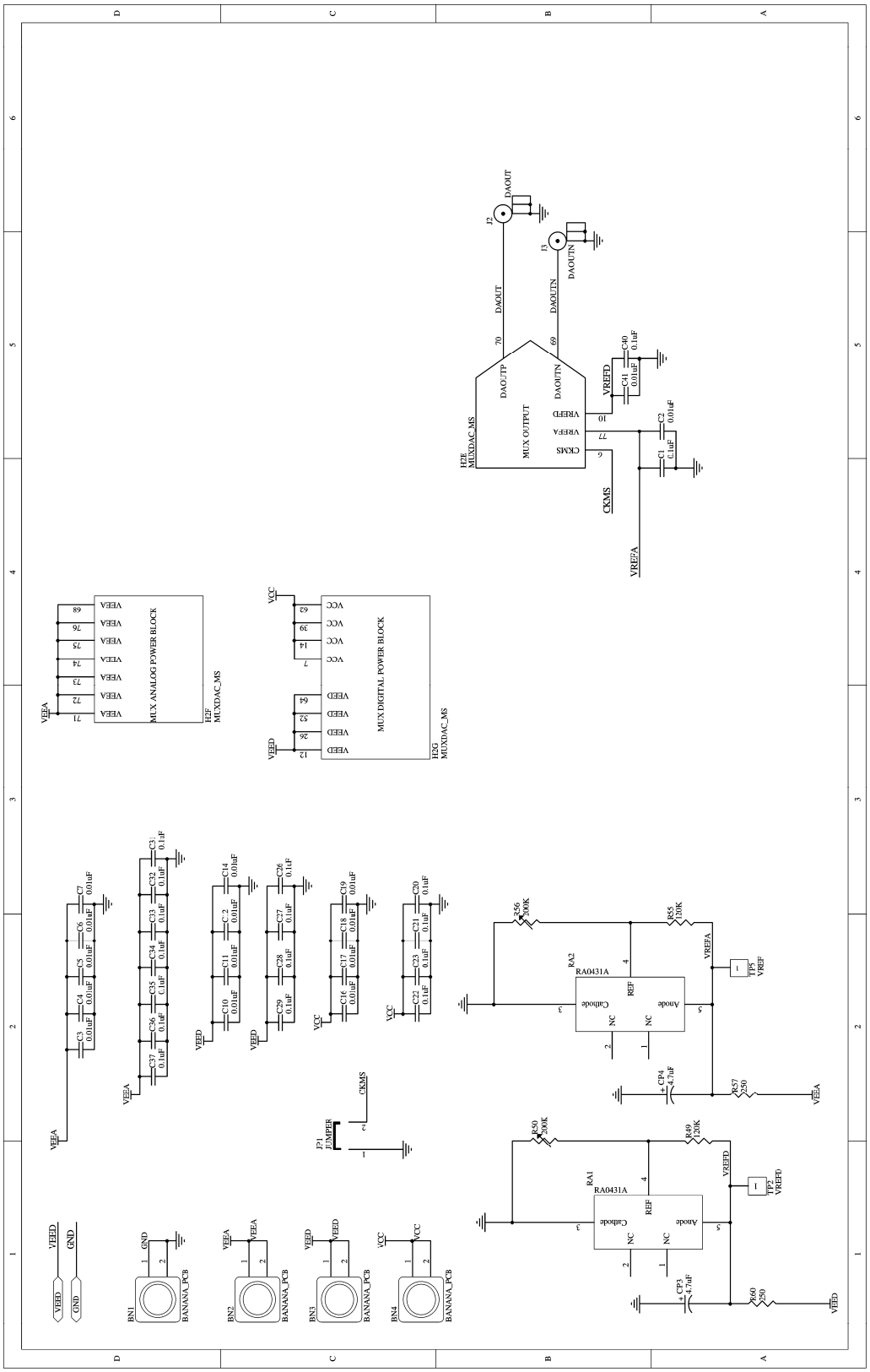

Figure 5 - EVRDA012M4MS schematics (2)

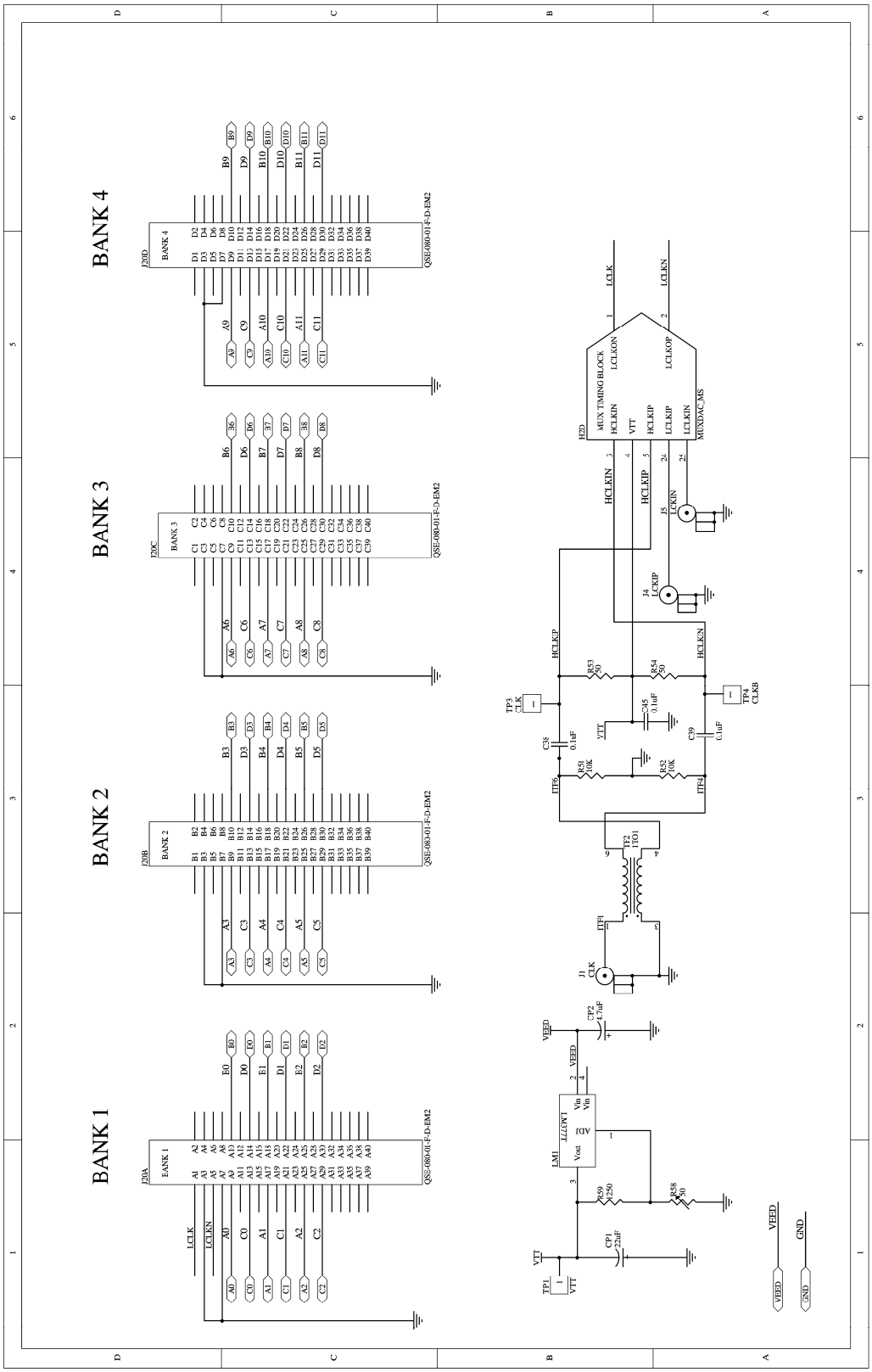

Figure 6 - EVRDA012M4MS schematics (3)

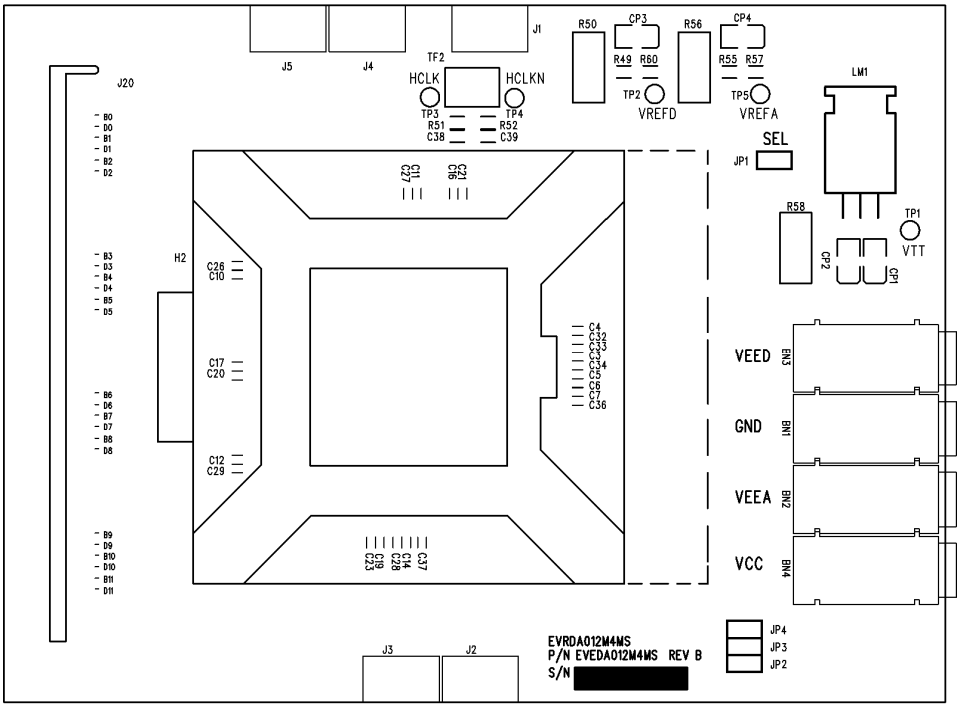

Figure 7 - Top layer stencil

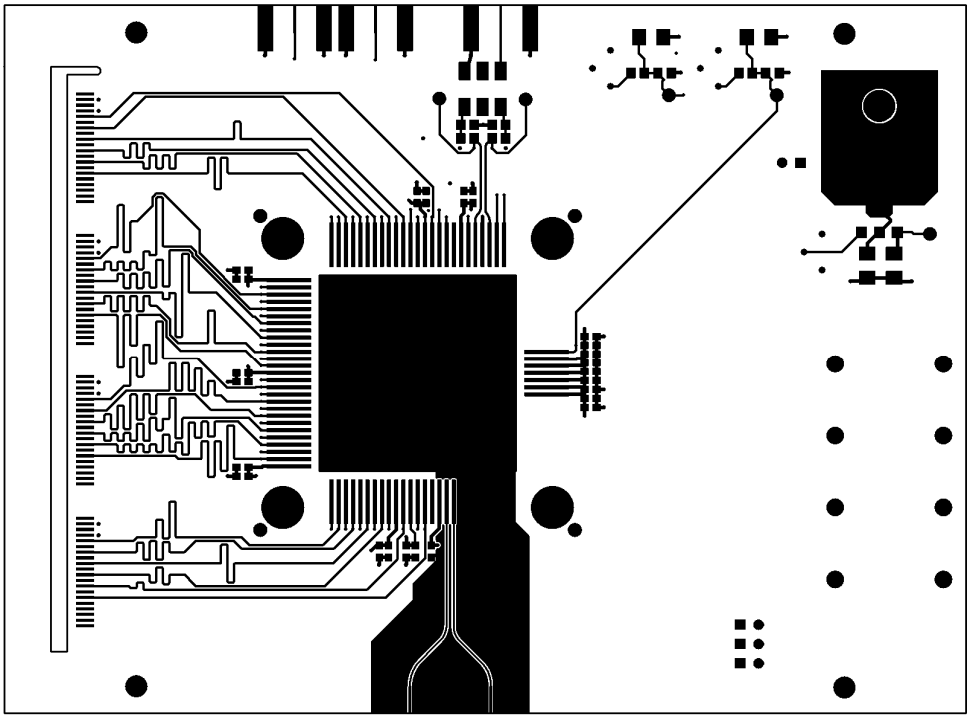

Figure 8 - Top layer

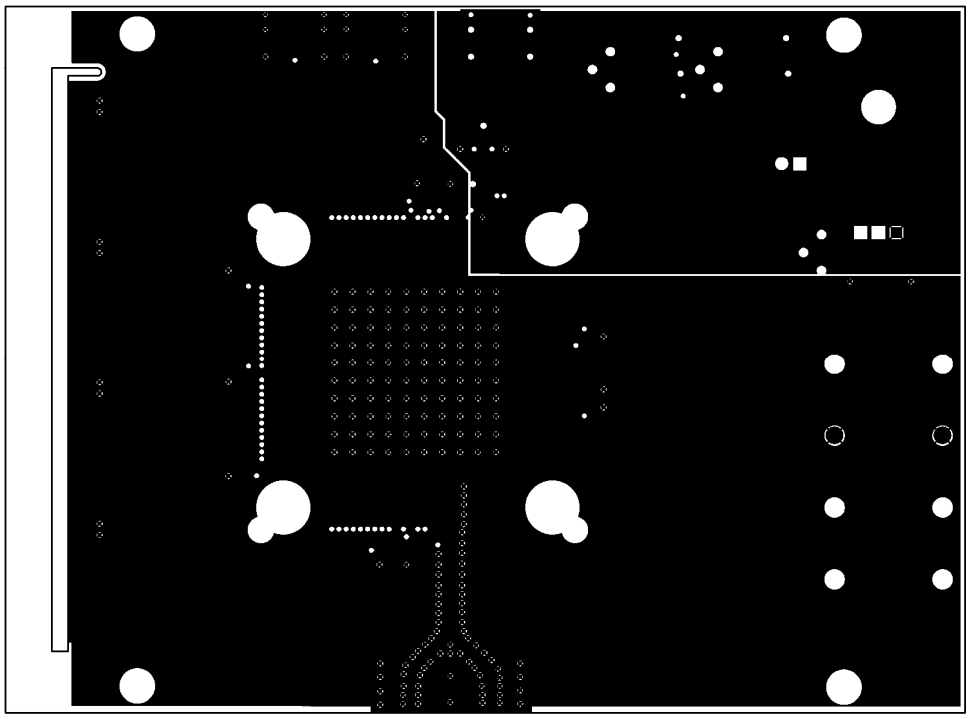

Figure 9 - GND

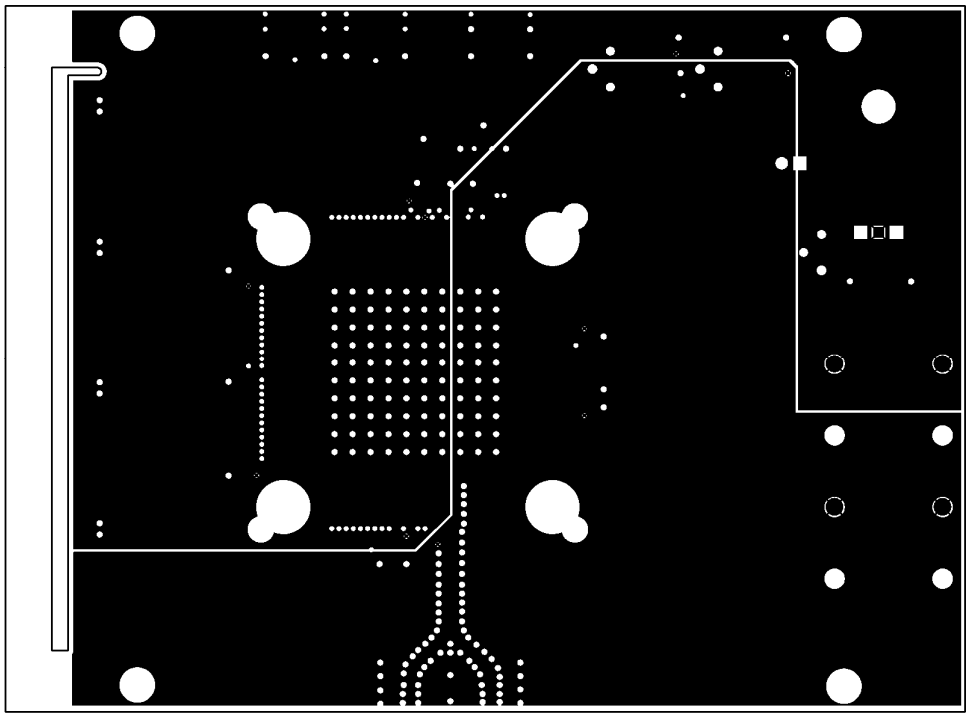

Figure 10 - VEEA and VEED

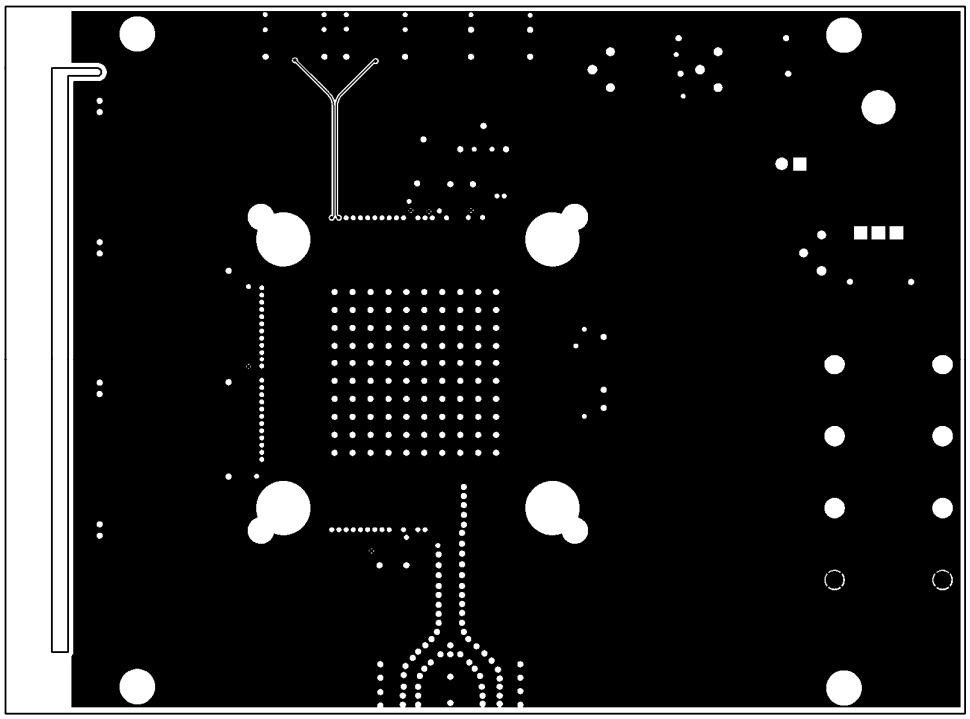

Figure 11 - VCC

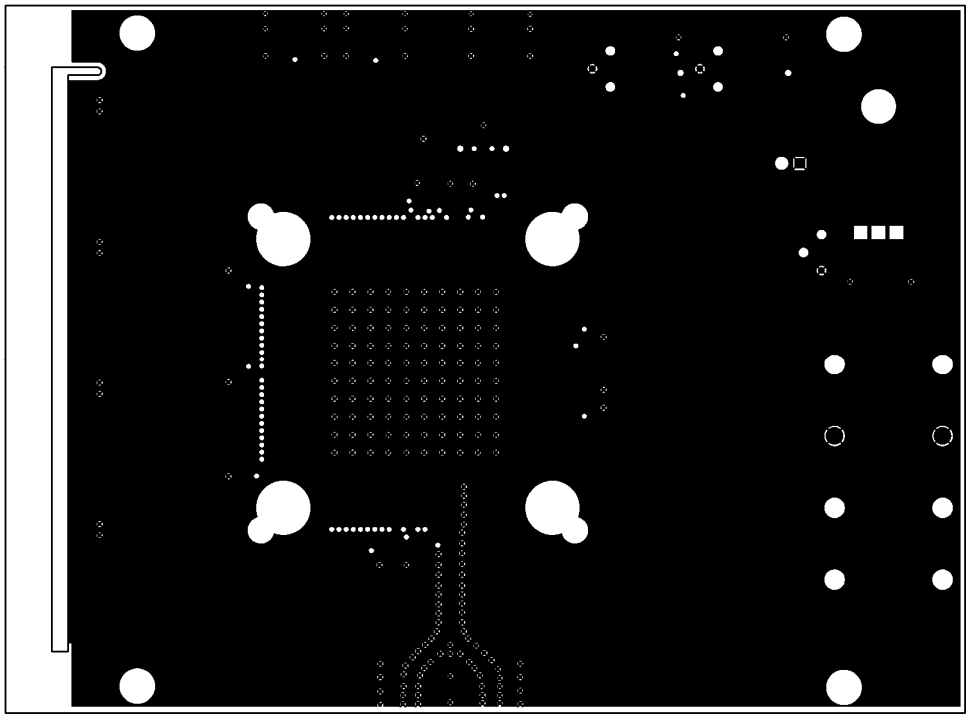

Figure 12 - GND

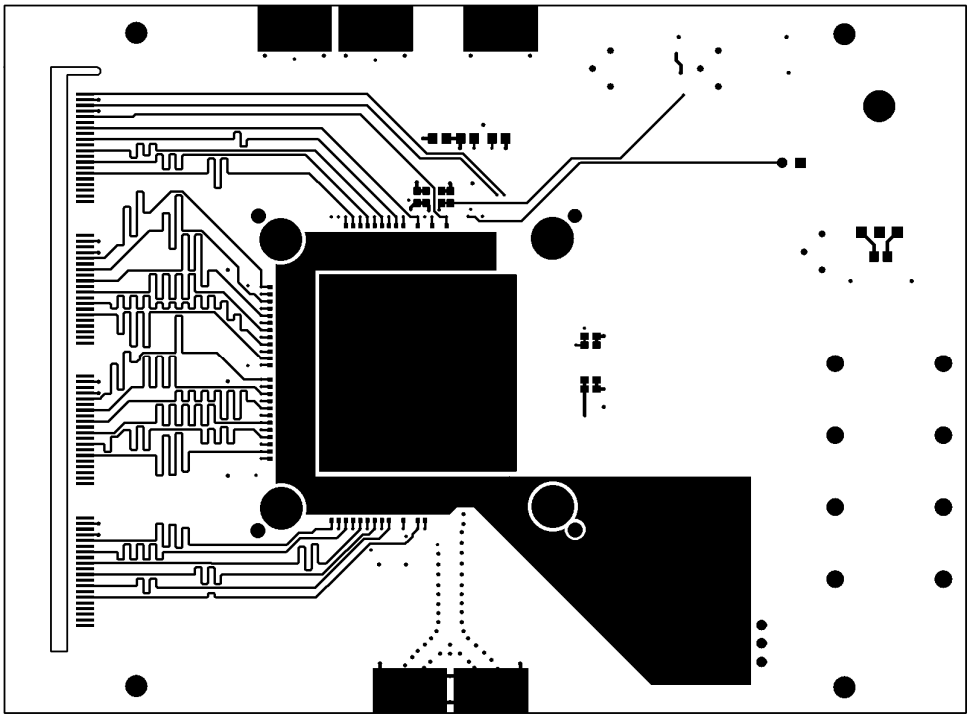

Figure 13 - Bottom layer

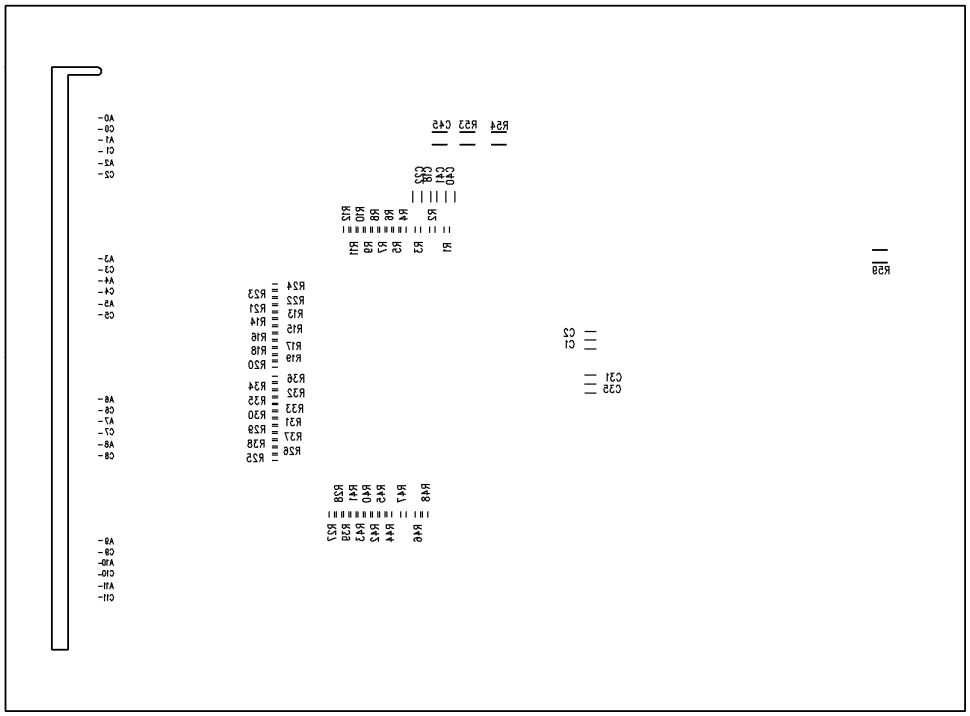

Figure 14 - Bottom layer stencil