TELEDYNE SCIENTIFIC COMPANY

EVRDA012RZ

12 Bit 1 GS/s Return-to-Zero DAC Evaluation Board

Features

- 2 mating board options for input: UHD or SMA
- On-Board Balun Conveniently Converts High-Speed Clock Input to Differential Clock
- Fully Assembled and Tested DAC for your evaluation and prototyping needs

Product Description

The EVRDA012RZ is an evaluation board designed to demonstrate the performance of the RDA012RZ (RZDAC), a 1GS/s, return-to-zero digital-to-analog converter IC. The return-to-zero feature of the RZDAC allows for operation in the 2nd Nyquist band. The evaluation kit consists of two assembled printed circuit boards: one hosting the RZDAC IC, and one the input connection.

There are two different input boards available, allowing the user to select SMA or UHD connectors. A third option is to use the Teledyne Scientifics' programmable data generator (RGA012M4) to supply the data. The data generator board allows the user to evaluate the RZDAC without any data generating equipment. Only a sampling clock input is required.

For added convenience, the input high speed clock is converted on board into a differential clock using a high-frequency balun.

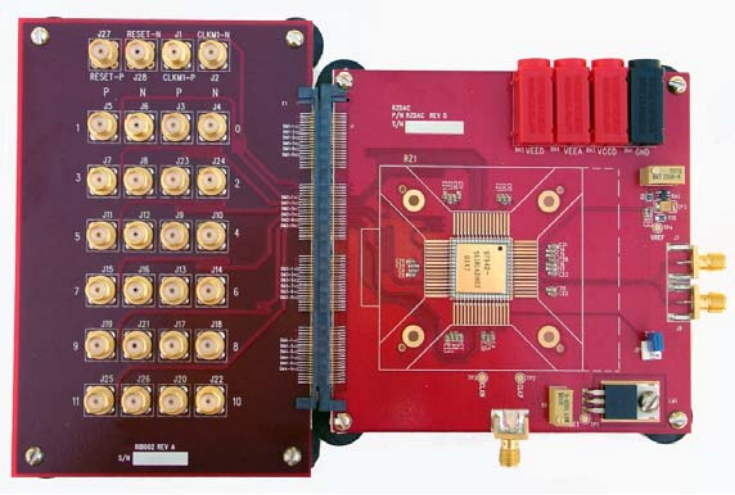

Figure 1 – EVRDA012RZ-QP-SMA

Ordering information

PART NUMBER	DESCRIPTION
EVRDA012RZ-QP-SMA	RDA012RZ-QP Evaluation Board w/ SMA Input Connection Board
EVRDA012RZ-QP-UHD	RDA012RZ-QP Evaluation Board w/ UHD Input Connection Board

Signal Description

Power Supplies

The evaluation board requires both a negative and positive supply voltage, and separate digital and analog supplies. VEEA is the analog –5.2V supply, VEED is the digital –5.2V supply. VCC is a +3.3V supply. Connect the power supplies to the evaluation board using banana cables. There is no need for power-up sequencing.

Inputs

The EVRDA012RZ has three mating options for input. For connector based data input, the user may choose the SMA connector mating board, or "UHD" (Ultra High Density from Gore) mating board. The third option is the Teledyne Scientifics' RGA012M4, a programmable FPGA-based data generator board. The data generator board allows users to program their own data vectors for the RZDAC to sample. All that must be provided is the external sampling clock for both EVRDA012RZ and RGA012M4. See the RGA012M4 user guide for more information.
The EVRDA012RZ data input is LVDS compatible with D11 being the input most significant bit (MSB) and D0 the least significant bit (LSB).

The default mode of the RZDAC IC is return-to-zero (RZ) operation. The jumper JP1 controls the TMS (Track-Mode-Select) signal, which in turn selects the RZDAC operation mode. Leave JP1 uncapped for RZ mode or jump it for conventional Nyquist DAC mode (Zero-Order-Hold DAC).
The input clock signal is supplied through an SMA connector, J6, and is converted into a differential signal through a high frequency balun. The differential clock can be checked at TP2 and TP3.
VREF is a –2V reference that is derived from the power supplies and made available to the RZDAC. Potentiometer R8 in this circuit may have to be adjusted to achieve the nominal –2V. A test points is provided for probing purposes. It is a good idea to check that VREF is nominally –2V after power up to achieve optimum performance from the RZDAC. Likewise, potentiometer R1 may need adjustment to ensure a VTT value of –1.3V, the termination voltage for the differential sampling clock.

Outputs

The analog output (OUTP, OUTN) of the RZDAC is available on the SMA connectors J7 & J8. OUTP and OUTN should be terminated with 50Ω impedance to ground.

PC Board Layout

The EVRDA012RZ is fabricated using six layers of Rogers 4350 material. Interface to the input board is through the QSE-080-01-F-D-EM2 high-speed edge connector from Samtec.

All data and clock signals are treated as 50Ω transmission lines. Figure 2 is the layer stack of the evaluation board, including layer thickness.

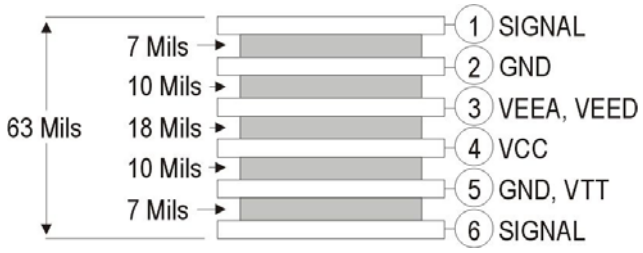

Figure 2 - EVRDA012RZ layer stack

Components

Table 1: Jumper and Test Point List

DESIGNATOR / SIGNAL	SETTINGS	FUNCTION
JP1 / TMS (Track-Mode-Select)	OFF: TMS is HIGH ON: Link TMS to GND	OFF: DAC in return-to-zero mode ON: DAC in zero order hold mode
TP1 / VTT	Nominally –1.3V	Test point
TP2 / CLKP	CLKP = positive sample clock	Test point
TP3 / CLKN	CLKN = negative sample clock	Test point
TP4 / VREF	Between –1.8V and –2.2V	Test point

Table 2: Component List

DESIGNATOR	QTY	DESCRIPTION
C1, C2, C3, C4, C6, C8, C10, C12, C14, C15, C16, C17, C20, C21, C26, C27, C30, C32, C35	19	0.1uF Capacitors (0603 size)
C5, C7, C9, C11, C13, C22, C23, C24, C28, C29, C31, C33, C34	13	0.01uF Capacitors (0603 size)
CP1, CP2, CP3, CP4, CP6, CP7	6	4.7uF Capacitors (TAJB475K016R)
R1	1	100Ω Potentiometer (64Y101)
R2	1	1250Ω Resistor
R3, R4	2	50Ω Resistor (0805 size)
R5, R6	2	10KΩ Resistor (0805 size)
R8	1	200KΩ Potentiometer (64Y204)
R9	1	120KΩ Resistor (0805 size)
R10	1	250Ω Resistor (0805 size)
TF1	1	Balun (ADTL2-18)
J1	1	Edge Connector (QSE-080-01-F-D-EM2)
J6, J7, J8	3	SMA Connector (142-0701-851)
BN1, BN2, BN3, BN4	4	Banana Plug Sockets
JP1	1	2 Pin Header
LM1	1	Adjustable Regulator (LM337)
RA1	1	Shunt Regulator (TLV431ASNT1)
RZ1	1	Return-to-Zero DAC (RDA012RZ)

Board Configuration

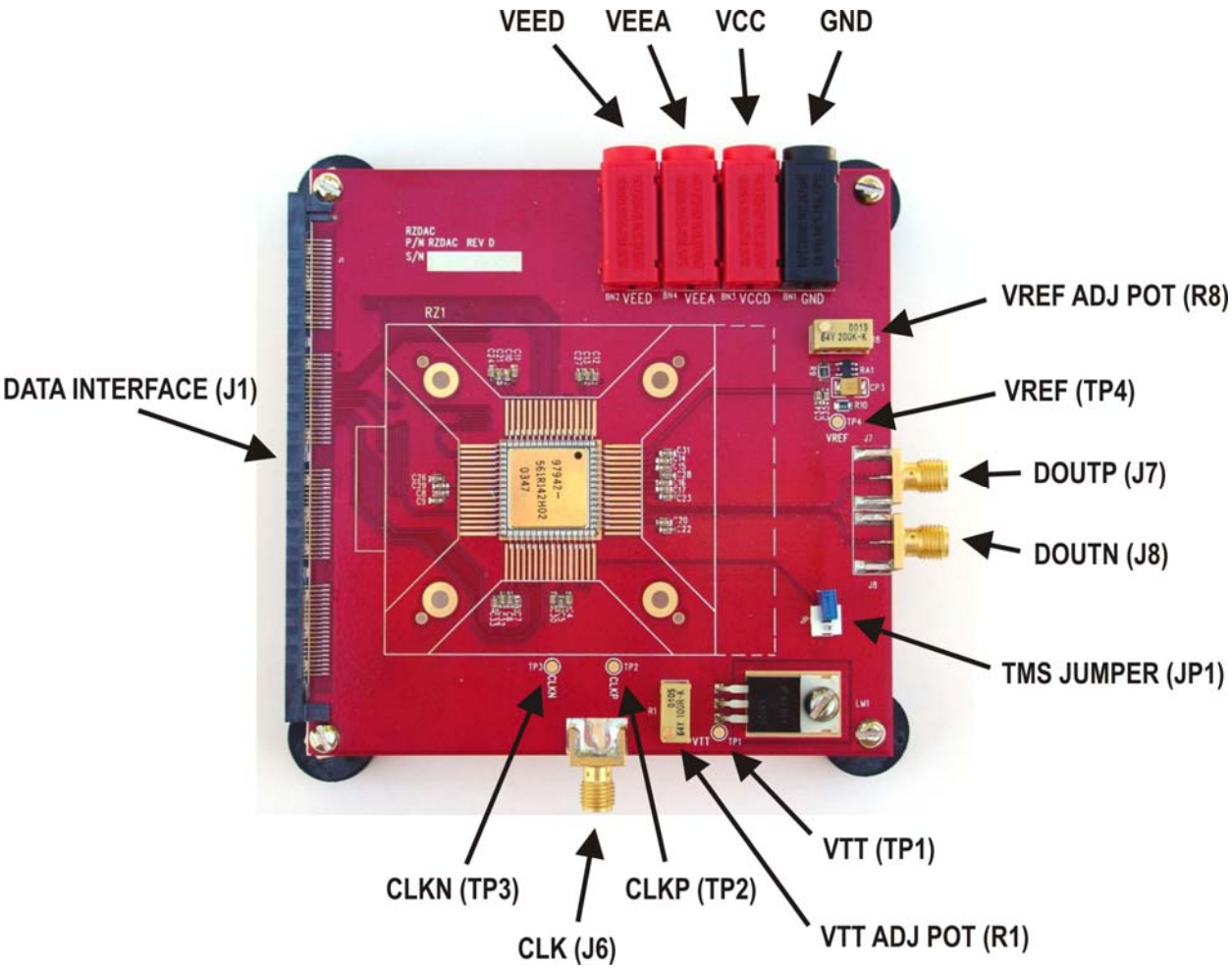

Figure 3 - EVRDA012RZ board configuration

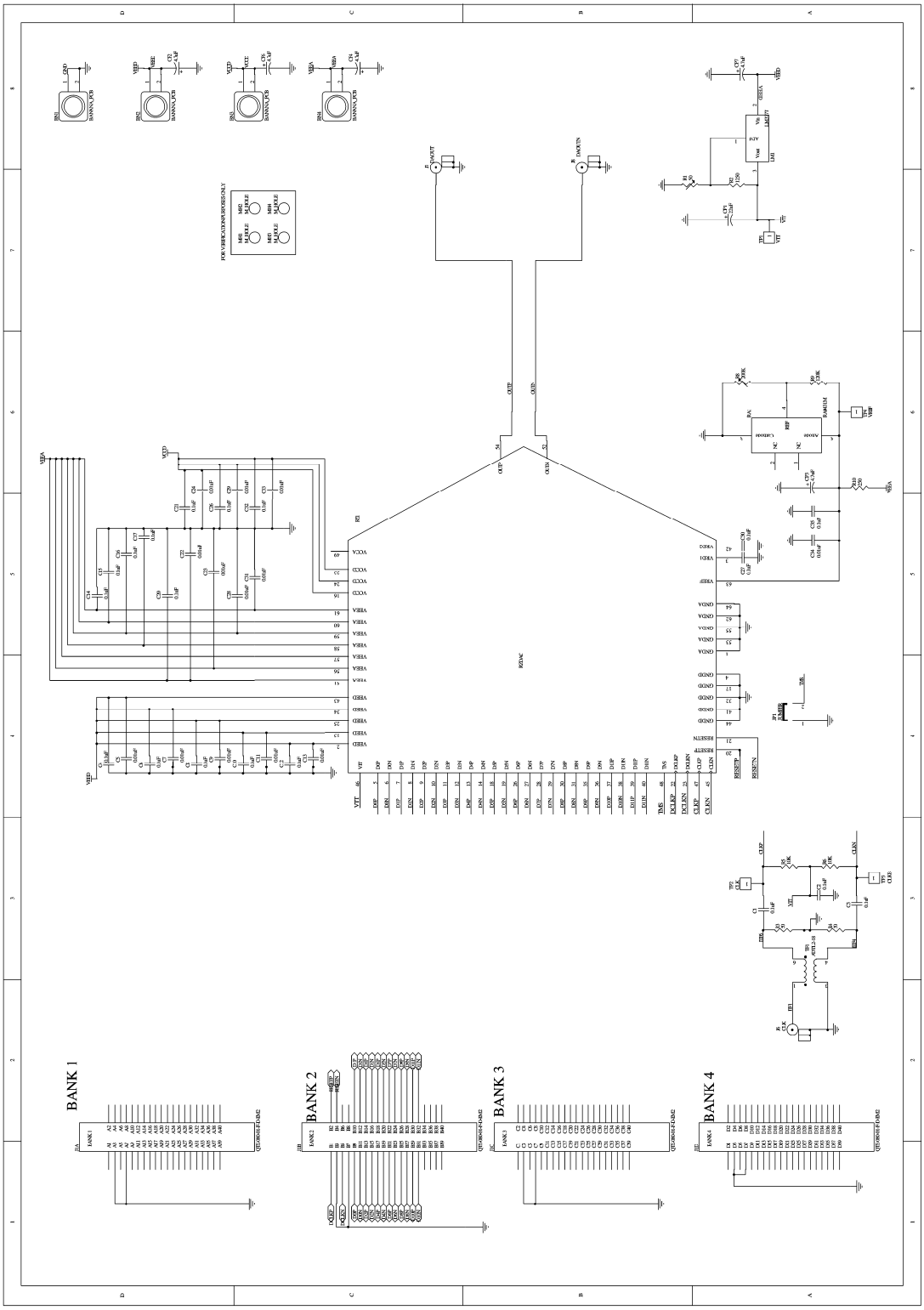

Figure 4 - EVRDA012RZ schematics

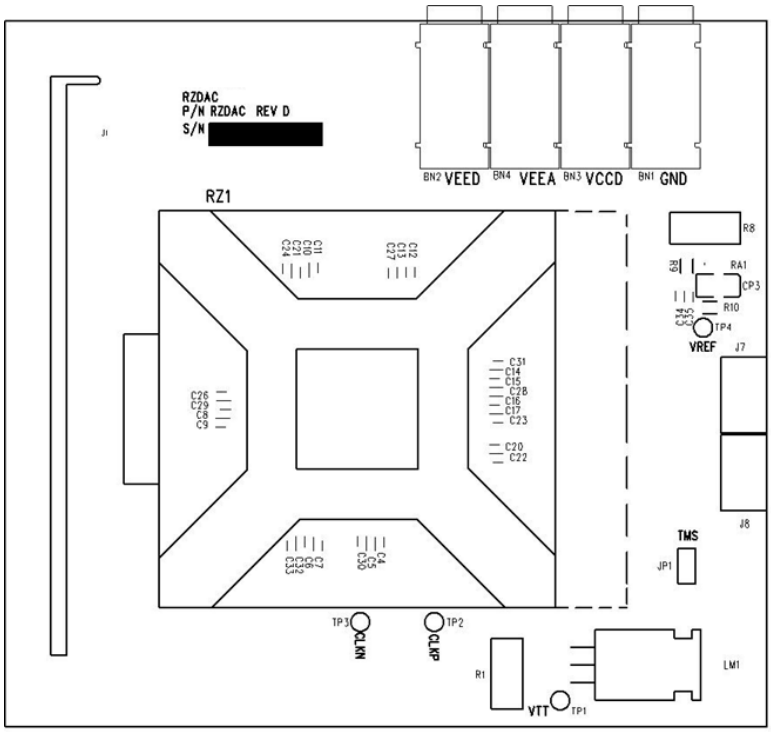

Figure 5 - Top layer stencil

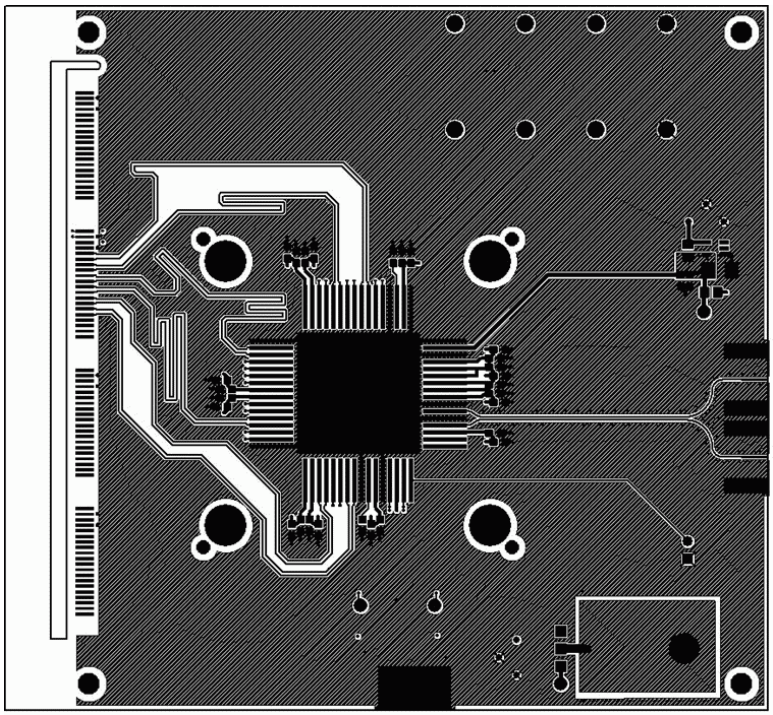

Figure 6 - Top layer

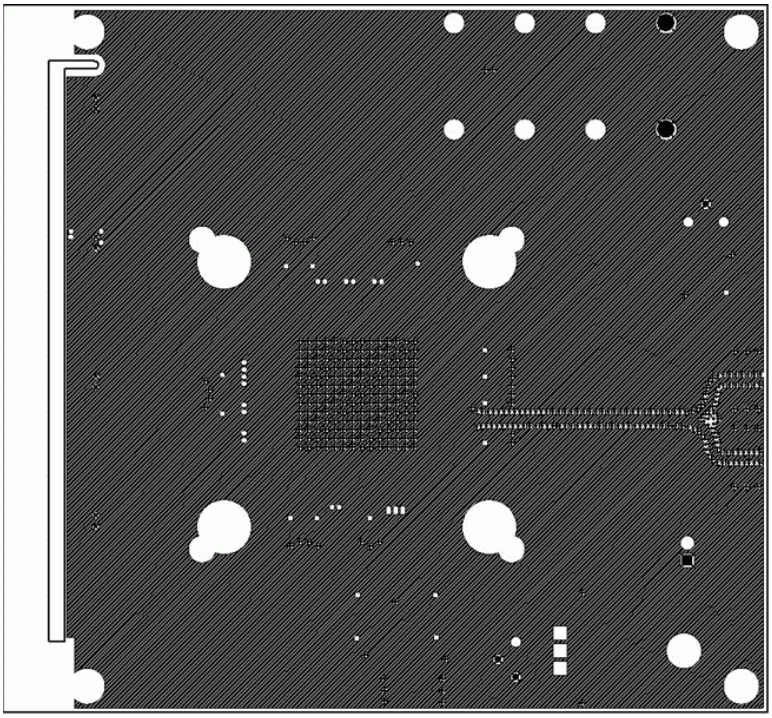

Figure 7 - GND

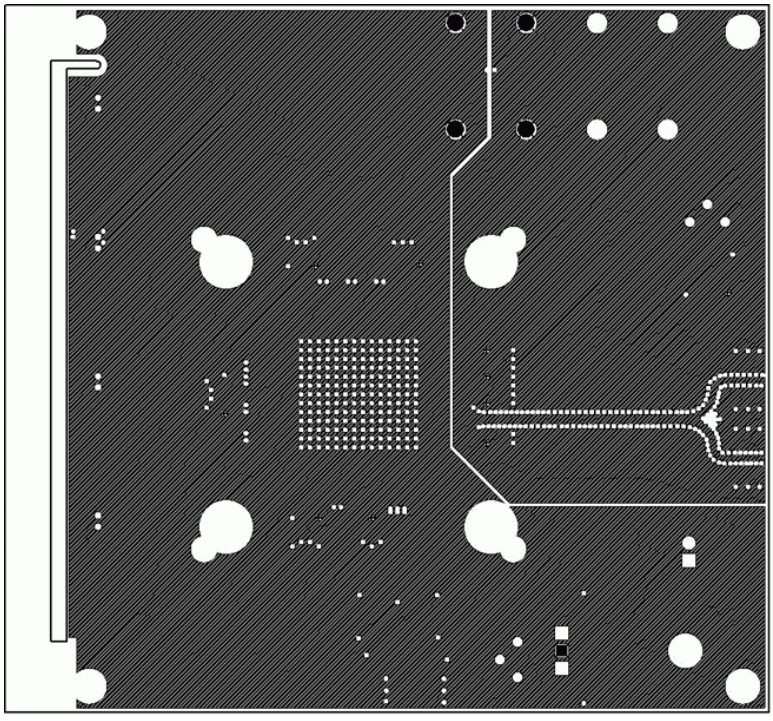

Figure 8 - VEEA and VEED

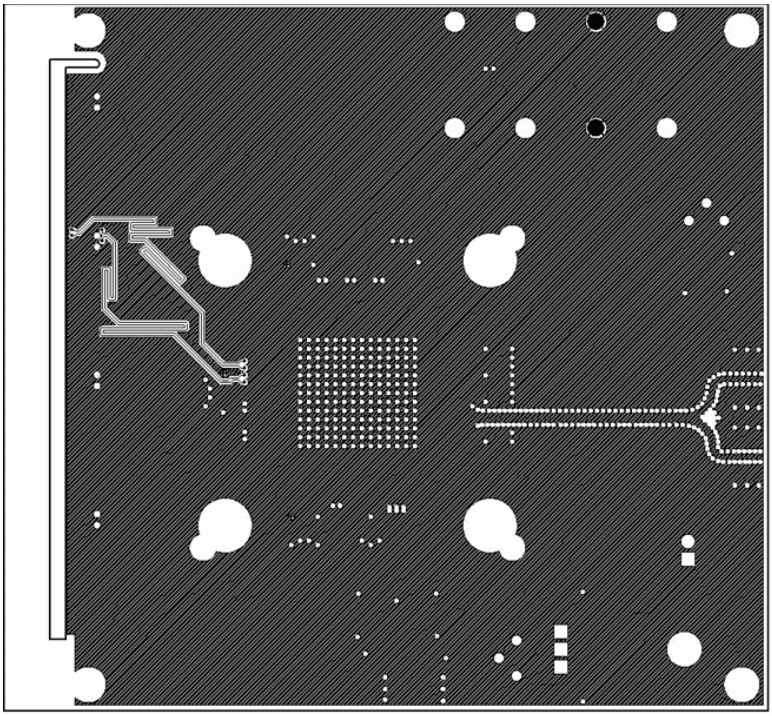

Figure 9 - VCC

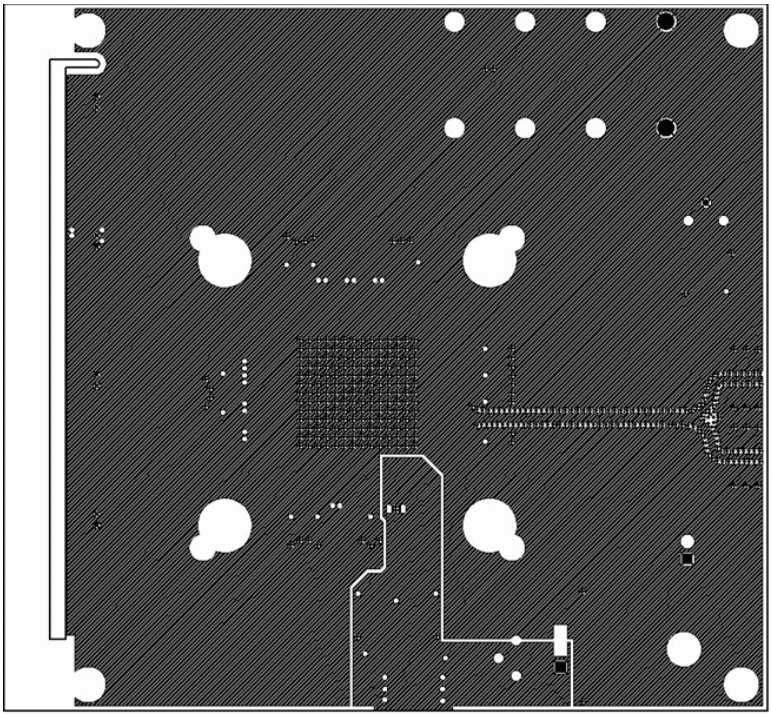

Figure 10 - GND

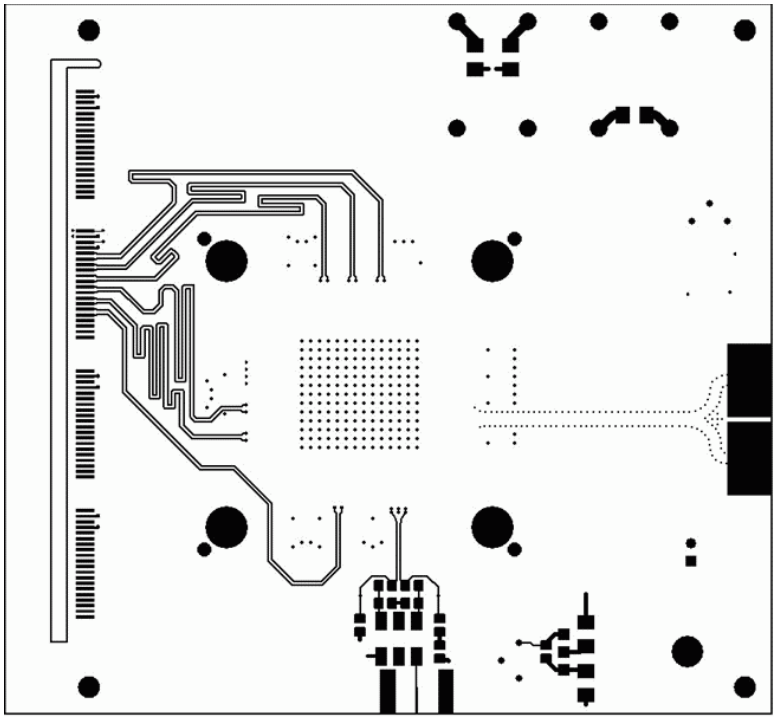

Figure 11 - Bottom layer

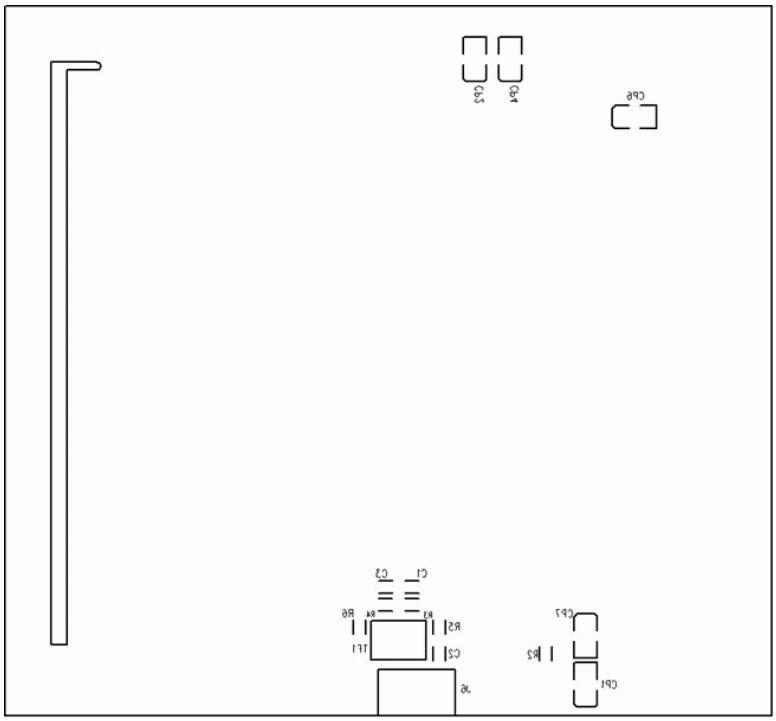

Figure 12 - Bottom layer stencil