TELEDYNE
SCIENTIFIC COMPANY

RTH040

11 GHz Bandwidth 1 GS/s Dual Track-and-Hold

REV-DATE PC4-2412
FILE DS_0026PC4-2412
DS

RTH040

11 GHz Bandwidth 1 GS/s Dual Track-and-Hold

Features

- 11 GHz Input Bandwidth (0.25 Vpp V_{IN} Differential)
- 100 - 1000 MHz Sampling Rate (TH1)
- 10 - 1000 MHz Output Data Rate (TH2)
- -76 dB Hold Mode Distortion
  (1.0 GHz 0.25 Vpp V_{IN} Differential)
- -56 dB Hold Mode Distortion
  (1.0 GHz 0.25 Vpp V_{IN} SE)
- -57 dB Hold Mode Distortion
  (4.0 GHz 0.25 Vpp V_{IN} Differential)
- -36 dB Hold Mode Distortion
  (4.0 GHz 0.25 Vpp V_{IN} SE)
- < 50 fs Aperture Jitter
- < 200 ps Acquisition Time
- < 25 ps Rise Time (20 - 80%)
- Differential Analog Input/Output
- Output Held more than Half Clock Cycle
- Track Mode Select

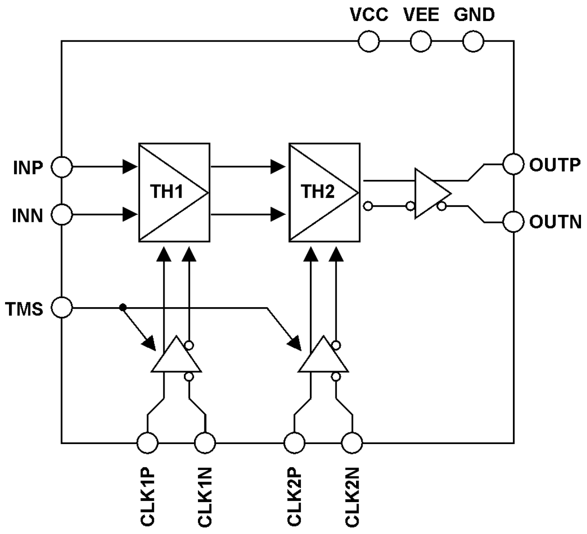

Figure 1. Functional Block Diagram

Product Description

RTH040's bandwidth and aperture jitter enable 1 GS/s accurate sampling of DC to multi-GHz signals. The differential-to-differential dual track-and-hold cascades two track-and-hold circuits, TH1 and TH2. The RTH040 provides a held output for more than half a clock cycle, easing bandwidth requirements of subsequent circuitry relative to the case of a single track-and-hold (TH). The option to independently clock TH1 and TH2 (as low as 10 MHz) further relaxes this requirement for sub-sampling applications.

Ordering information

PART NUMBER	DESCRIPTION
RTH040-QP	24 Pin QFP Package
RTH040-DI	Die
EVRTH040-QP	Evaluation Board with a RTH040-QP

CAUTION

DEVICE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)

Absolute Maximum Ratings

Supply Voltages

VCC to GND	-1 to +6 V
VEE to GND	-6 to +1 V
VCC to VEE	-1 to +11 V

Input Voltages

INP, INN to GND	-1 to +1 V
CLK1P, CLK1N, CLK2P, CLK2N to GND	-1 to +1 V
TMS to GND	-6 to +1 V

Output Voltages

Vterm (Output Termination Voltage) to GND	-2.5 to +0.5V

Temperature

Case Temperature	-15 to +85 °C
Junction Temperature	+125 °C
Lead, Soldering (10 Seconds)	+220 °C
Storage	-40 to 125 °C

DC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VCC = 5V; VEE = -5.2V; Clocks: 1GHz, 0.6Vpp Differential; Input: 250mV Single-Ended; Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
1.0	**DC TRANSFER FUNCTION**						
1.1	Gain	G		-3.0		-2.3	dB
1.2	Offset Voltage	V_{OFF}	Absolute Value			18	mV
1.3	Common-Mode Rejection	CMRR	0.25 Vpp at INP and INN, in phase		-60		dB
2.0	**TEMPERATURE DRIFT**						
2.1	Warm-up Time		After Power-up			10	s
2.2	Gain Drift		After Warm-up, from 20°C to 120°C		740		ppm/°C
2.3	Offset Voltage Drift		After Warm-up, from 20°C to 120°C		7		µV/°C
3.0	**ANALOG INPUT (INP, INN)**						
3.1	Input Resistance	R_{IIN}	Each Lead to GND	46	50	54	Ω
3.2	Input Capacitance	C_{IIN}	Each Lead to GND			300	fF
4.0	**CLOCK INPUTS (CLK1P, CLK1N, CLK2P, CLK2N)**						
4.1	Input Resistance	R_{CIN}	Each Lead to GND	46	50	54	Ω
4.2	Input Capacitance	C_{CIN}	Each Lead to GND			300	fF
5.0	**DIGITAL INPUT (TMS)**						
5.1	Current Draw		Into Lead, High		0.75		mA
6.0	**ANALOG OUTPUT (OUTP, OUTN)**						
6.1	Common Mode Voltage	OUT_{CM}	Relative to Vterm	-0.7	-0.6	-0.5	V
6.2	Average Current		Into Each Output Lead		12		mA
6.3	Maximum Current		Into Output Lead		20		mA
7.0	**INPUT-OUTPUT ISOLATION**						
7.1	TH1 Hold, TH2 Track		9 GHz 0.5 Vpp input		39		dB
7.2	TH1 Track, TH2 Hold		9 GHz 0.5 Vpp input		41		dB
7.3	TH1 Hold, TH2 Hold		9 GHz 0.5 Vpp input		39		dB
8.0	**POWER SUPPLY REQUIREMENTS**						
8.1	Positive Supply Current	ICC			80		mA
8.2	Negative Supply Current	IEE			230		mA
8.3	Power Dissipation	P			1.6	1.9	W

AC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VCC = 5V; VEE = -5.2V; Clocks: 1GHz, 0.6Vpp Differential; Input: 250mV Single-Ended; Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
9.0	**DYNAMIC TRACK MODE PERFORMANCE, SINEWAVE INPUT**						
9.1	Track Bandwidth		-3dB Gain, TH1 & TH2 In Track Mode		1000		MHz
9.2	Gain Flatness Deviation					±0.5	dB
9.3	Integrated Noise		Input Referred		800		μV
9.4	Noise Floor		Input Referred		6.7		nV/√Hz
10.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT**						
10.1	Gain Flatness Deviation	GFD	From DC to 6GHz			±1	dB
10.2	Integrated Noise		Input Referred			1600	μV
10.3	Noise Floor		Input Referred			10	nV/√Hz
10.4	TH1 Hold Feedthrough[1]		500 MHz 1 Vpp Input		-72		dB
10.5	TH1 Hold Feedthrough[6]		1 GHz 1 Vpp Input		-68		dB
11.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.25Vpp DIFFERENTIAL**						
11.1	Bandwidth	BW_L	-3dB Gain, 0.25 V_{PP} Differential	11	11		GHz
11.2	SFDR 60 MHz	SFDR1	0.25 Vpp Differential Input	79	80		dB
11.3	SFDR 1060 MHz	SFDR2	0.25 Vpp Differential Input	75	78		dB
11.4	SFDR 2060 MHz	SFDR3	0.25 Vpp Differential Input	72	75		dB
11.5	SFDR 3060 MHz	SFDR4	0.25 Vpp Differential Input	65	68		dB
11.6	SFDR 4060 MHz	SFDR5	0.25 Vpp Differential Input	56	58		dB
11.7	SFDR 5060 MHz	SFDR6	0.25 Vpp Differential Input	54	57		dB
11.8	SFDR 6060 MHz	SFDR7	0.25 Vpp Differential Input	49	53		dB
11.9	SFDR 7060 MHz	SFDR8	0.25 Vpp Differential Input	47	50		dB
11.10	SFDR 8060 MHz	SFDR9	0.25 Vpp Differential Input	40	42		dB
11.11	SFDR 9060 MHz	SFDR10	0.25 Vpp Differential Input	45	48		dB
11.12	SFDR 10060 MHz	SFDR11	0.25 Vpp Differential Input	47	51		dB
11.13	SFDR 11060 MHz	SFDR12	0.25 Vpp Differential Input	44	47		dB
11.14	SFDR 12060 MHz	SFDR13	0.25 Vpp Differential Input	48	51		dB
11.15	THD 60 MHz	THD1	0.25 Vpp Differential Input	-76	-77		dB
11.16	THD 1060 MHz	THD2	0.25 Vpp Differential Input	-74	-76		dB
11.17	THD 2060 MHz	THD3	0.25 Vpp Differential Input	-71	-73		dB
11.18	THD 3060 MHz	THD4	0.25 Vpp Differential Input	-63	-65		dB
11.19	THD 4060 MHz	THD5	0.25 Vpp Differential Input	-55	-57		dB
11.20	THD 5060 MHz	THD6	0.25 Vpp Differential Input	-53	-55		dB
11.21	THD 6060 MHz	THD7	0.25 Vpp Differential Input	-49	-51		dB
11.22	THD 7060 MHz	THD8	0.25 Vpp Differential Input	-47	-49		dB
11.23	THD 8060 MHz	THD9	0.25 Vpp Differential Input	-40	-42		dB
11.24	THD 9060 MHz	THD10	0.25 Vpp Differential Input	-44	-47		dB
11.25	THD 10060 MHz	THD11	0.25 Vpp Differential Input	-47	-50		dB
11.26	THD 11060 MHz	THD12	0.25 Vpp Differential Input	-44	-46		dB
11.27	THD 12060 MHz	THD13	0.25 Vpp Differential Input	-47	-49		dB

---

[1] Measured with TH2 in track mode and comparing the DTH output for TH1 in track and hold mode. See Theory of Operation.

Test Conditions (see notes for specific conditions): Room Temperature; VCC = 5V; VEE = -5.2V; Clocks: 1GHz, 0.6Vpp Differential; Input: 250mV Single-Ended; Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
12.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.5Vpp DIFFERENTIAL**						
12.1	Bandwidth	BW_M	-3dB Gain, 0.5 V_{PP} Differential	11	11		GHz
12.2	SFDR 60 MHz	SFDR14	0.5 Vpp Differential Input	83	87		dB
12.3	SFDR 1060 MHz	SFDR15	0.5 Vpp Differential Input	68	72		dB
12.4	SFDR 2060 MHz	SFDR16	0.5 Vpp Differential Input	66	69		dB
12.5	SFDR 3060 MHz	SFDR17	0.5 Vpp Differential Input	55	57		dB
12.6	SFDR 4060 MHz	SFDR18	0.5 Vpp Differential Input	51	53		dB
12.7	SFDR 5060 MHz	SFDR19	0.5 Vpp Differential Input	46	48		dB
12.8	SFDR 6060 MHz	SFDR20	0.5 Vpp Differential Input	43	46		dB
12.9	SFDR 7060 MHz	SFDR21	0.5 Vpp Differential Input	40	42		dB
12.10	SFDR 8060 MHz	SFDR22	0.5 Vpp Differential Input	36	38		dB
12.11	SFDR 9060 MHz	SFDR23	0.5 Vpp Differential Input	42	44		dB
12.12	SFDR 10060 MHz	SFDR24	0.5 Vpp Differential Input	44	46		dB
12.13	SFDR 11060 MHz	SFDR25	0.5 Vpp Differential Input	39	41		dB
12.14	SFDR 12060 MHz	SFDR26	0.5 Vpp Differential Input	43	45		dB
12.15	THD 60 MHz	THD14	0.5 Vpp Differential Input	-81	-83		dB
12.16	THD 1060 MHz	THD15	0.5 Vpp Differential Input	-68	-71		dB
12.17	THD 2060 MHz	THD16	0.5 Vpp Differential Input	-66	-68		dB
12.18	THD 3060 MHz	THD17	0.5 Vpp Differential Input	-54	-56		dB
12.19	THD 4060 MHz	THD18	0.5 Vpp Differential Input	-48	-50		dB
12.20	THD 5060 MHz	THD19	0.5 Vpp Differential Input	-44	-46		dB
12.21	THD 6060 MHz	THD20	0.5 Vpp Differential Input	-41	-43		dB
12.22	THD 7060 MHz	THD21	0.5 Vpp Differential Input	-40	-41		dB
12.23	THD 8060 MHz	THD22	0.5 Vpp Differential Input	-36	-37		dB
12.24	THD 9060 MHz	THD23	0.5 Vpp Differential Input	-39	-41		dB
12.25	THD 10060 MHz	THD24	0.5 Vpp Differential Input	-41	-44		dB
12.26	THD 11060 MHz	THD25	0.5 Vpp Differential Input	-38	-40		dB
12.27	THD 12060 MHz	THD26	0.5 Vpp Differential Input	-41	-43		dB
13.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 1Vpp DIFFERENTIAL**						
13.1	Bandwidth	BW_H	-3dB Gain, 1 V_{PP} Differential	9	9		GHz
13.2	SFDR 60 MHz	SFDR27	1 Vpp Differential Input	76	77		dB
13.3	SFDR 1060 MHz	SFDR28	1 Vpp Differential Input	61	64		dB
13.4	SFDR 2060 MHz	SFDR29	1 Vpp Differential Input	60	63		dB
13.5	SFDR 3060 MHz	SFDR30	1 Vpp Differential Input	42	44		dB
13.6	SFDR 4060 MHz	SFDR31	1 Vpp Differential Input	42	43		dB
13.7	SFDR 5060 MHz	SFDR32	1 Vpp Differential Input	38	39		dB
13.8	SFDR 6060 MHz	SFDR33	1 Vpp Differential Input	32	34		dB
13.9	SFDR 7060 MHz	SFDR34	1 Vpp Differential Input	36	37		dB
13.10	SFDR 8060 MHz	SFDR35	1 Vpp Differential Input	34	35		dB
13.11	SFDR 9060 MHz	SFDR36	1 Vpp Differential Input	36	37		dB
13.12	SFDR 10060 MHz	SFDR37	1 Vpp Differential Input	39	40		dB
13.13	THD 60 MHz	THD27	1 Vpp Differential Input	-73	-75		dB
13.14	THD 1060 MHz	THD28	1 Vpp Differential Input	-61	-63		dB
13.15	THD 2060 MHz	THD29	1 Vpp Differential Input	-58	-60		dB
13.16	THD 3060 MHz	THD30	1 Vpp Differential Input	-42	-43		dB
13.17	THD 4060 MHz	THD31	1 Vpp Differential Input	-41	-42		dB
13.18	THD 5060 MHz	THD32	1 Vpp Differential Input	-36	-37		dB
13.19	THD 6060 MHz	THD33	1 Vpp Differential Input	-30	-31		dB
13.20	THD 7060 MHz	THD34	1 Vpp Differential Input	-33	-34		dB
13.21	THD 8060 MHz	THD35	1 Vpp Differential Input	-31	-32		dB
13.22	THD 9060 MHz	THD36	1 Vpp Differential Input	-34	-35		dB
13.23	THD 10060 MHz	THD37	1 Vpp Differential Input	-36	-38		dB

Test Conditions (see notes for specific conditions): Room Temperature; VCC = 5V; VEE = -5.2V; Clocks: 1GHz, 0.6Vpp Differential; Input: 250mV Single-Ended; Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
14.0	**TRACK TO HOLD SWITCHING AND HOLD STATE, TH1**						
14.1	Aperture Delay	ta	After V(CLK1P) - V(CLK1N) Goes Neg.		50		ps
14.2	Aperture Jitter	Δt	Jitter Free 1-GHz 0.5-Vpp CLK1[2,3]		30		fs
14.3	Settling Time to 1 mV	ts	At Hold Capacitors. ttrack1,min Observed		250		ps
14.4	Differential Pedestal/V_{IN}[4]				-3		%
14.5	Diff. Droop Rate/V_{IN}				-1.5		%/ns
14.6	Hold Noise[5]		Per Sqrt (Hold Time)			50	µV/√ns
14.7	Maximum Hold Time[6]	$t_{HD1,MAX}$		5	8		ns
15.0	**HOLD TO TRACK SWITCHING AND TRACK STATE, TH1**						
15.1	Acquisition Time to 1 mV[7]	tacq	At Hold Caps, FSR Step At Input		200		ps
15.2	Max. Acq. Slew Rate	Dvdt,max	At Hold Caps, FSR Step At Input		12		V/ns
15.3	Rise Time	tr1	20 – 80%, 0.5Vpp input, defined at the sampling bridge.			25	ps
		tr2	20 – 80%, 1.0Vpp input, defined at the sampling bridge.		30		ps
15.4	Minimum Track Time	$t_{TR1,MIN}$			0.4		ns
15.5	Recovery Time		Required Accumulated Track Time After $t_{HD1,MAX}$ Violation			4	ns
16.0	**TRACK TO HOLD SWITCHING AND HOLD STATE, TH2**						
16.1	Aperture Delay	ta2	After V(CLK2P) - V(CLK2N) Goes Neg.		60		ps
16.2	Settling Time to 1 mV[8]	ts2	At DTH Output. ttrack2,min Observed		1000		ps
16.3	Differential Pedestal/V_{IN}[9]				0.25		%
16.4	Diff. Droop Rate/V_{IN}				-0.05		%/ns
16.5	Hold Noise		Per Sqrt (Hold Time)		25		µV/√ns
16.6	Maximum Hold Time	$t_{HD2,MAX}$		50			ns
17.0	**HOLD TO TRACK SWITCHING AND TRACK STATE, TH2**						
17.1	Minimum Track Time	$t_{TR2,MIN}$	After TH1 in Hold Mode	0		0.4	ns
17.2	Recovery Time		Required Accumulated Track Time After thold2,max Violation			4	ns

---

[2] The clock source jitter and the aperture jitter combine in an rms manner to yield the total sampling jitter. See Definition of Terms.

[3] Device aperture jitter increases as the V(CLK1P) – V(CLK1N) slew rate at the zero crossing decreases. See Theory of Operation.

[4] The differential pedestal error is proportional to the input signal. This gain loss may be observed at the DTH output if TH2 is in track mode during the TH1 track to hold transition.

[5] The variance of the hold noise is proportional to the hold time, thold. TH1 and TH2 hold noise, up to the output sampling instant, should be RMS added to the hold mode integrated noise of the DTH.

[6] Maximum hold time is determined by droop of single-ended hold capacitor voltages. The resulting shift of internal operating voltages is not directly observable at the DTH outputs but eventually causes device performance degradation.

[7] TH1 tacq, dvdt,max, and tr also apply to the reconstructed DTH output if sub-sampling a fast-edge repetitive wave form.

[8] Output is settled ta2 + ts2 after CLK2(P/N) downward transition.

[9] The differential pedestal error is proportional to the input signal.

Operating Conditions

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
18.0	**CLOCK INPUTS (CLK1P, CLK1N, CLK2P, CLK2N)**						
18.1	Amplitude[10]	V_{CPP}		200	600	1000	mVpp
18.2	Common Mode Voltage	V_{CCM}		-250	0	250	mV
18.3	CLK1 Frequency	F_{CLK1}		100		1000	MHz
18.4	CLK2 Frequency	F_{CLK2}		10		1000	MHz
19.0	**ANALOG INPUT (INP, INN)**						
19.1	Full Scale Range	FSR				1500	mVpp
19.2	Common Mode Voltage	V_{CM}		-100	0	100	mV
20.0	**DIGITAL INPUT (TMS)**						
20.1	Input High Voltage	V_{IH}		-0.5	0	1	V
20.2	Input Low Voltage	V_{IL}	Open TMS ≈ –1.4V	-1.5	Open	-1.2	V
21.0	**ANALOG OUTPUT (OUTP, OUTN)**						
21.1	Ext. Termination Voltage	V_{TERM}		0	0	0.5	V
21.2	Ext. Termination Resistor	R_{TERM}	Required From Outputs To Vterm		50		Ω
22.0	**POWER SUPPLY REQUIREMENTS**						
22.1	Positive Supply Voltage	VCC		4.75	5.0	5.25	V
22.2	Negative Supply Voltage	VEE		-5.45	-5.2	-4.95	V
23.0	**OPERATING TEMPERATURE[11]**						
23.1	Case Temperature	Tc	Measured at Bottom Plate	-15		85	°C
23.2	Junction Temperature	Tj				125	°C

---

[10] For > 500 MHz sinusoidal CLK1(P/N), 500 to 700 mVpp amplitude is recommended for combined aperture jitter and clock feed-through performance. At lower clock frequencies, use high amplitude for minimum jitter. See Theory of Operation.

[11] The part is designed to function within a junction temperature range of -40 ~ 125°C. For the best performance, operation within the specified temperature range with a proper heatsink attached to the device is recommended. The heatsink should be attached to the bottom of the PCB, on a metal pad connect by thermal vias to the metal pad where the part is soldered.

Pin Description and Pin Out

P/I/O	NAME	FUNCTION
P	GND	Power Supply Ground
P	VCC	Positive Power Supply, +5.0V
P	VEE	Negative Power Supply, -5.2V
I	CLK1P	Clock 1 Input: High = TH1 in Track Mode Low = TH1 in Hold Mode
I	CLK1N	Complementary Clock 1 Input
I	CLK2P	Clock 2 Input: High = TH2 in Track Mode Low = TH2 in Hold Mode
I	CLK2N	Complementary Clock 2 Input
I	INP	Analog Input
I	INN	Complementary Analog Input
I	TMS	Track Mode Select: Open = Sampled operation Ground = TH1 and TH2 in Track Mode
O	OUTP	Analog Output
O	OUTN	Complementary Analog Output

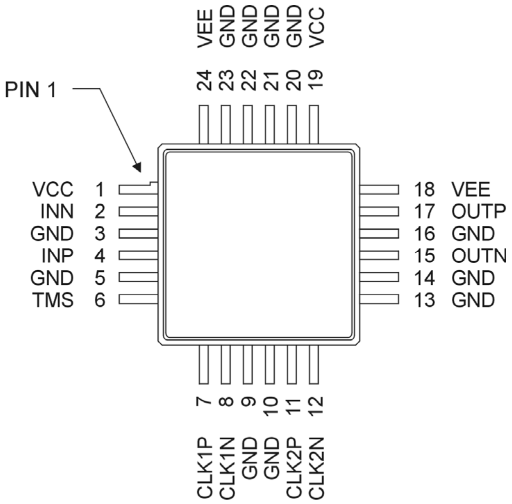

Figure 2. RTH040-QP pin configuration (top view, not to scale) 24-lead Quad Flat Package (QFP).

Definitions of Terms

Acquisition Time (tacq). The delay between the time a track-and-hold circuit (TH) enters track mode and the time the TH hold capacitor nodes track the input within some specified precision. The acquisition time sets a lower limit on the required track time during clocked operation.

Aperture Delay (ta). The average (or mean value) of the delay between the hold command (input clock switched from hold to track state) and the instant at which the analog input is sampled. The time is positive if the clock path delay is longer than the signal path delay. It is negative if the signal path delay is longer than the clock path delay.

Aperture Jitter (∆t). The standard deviation of the delay between the hold command (input clock switched from track-to-hold state) and the instant at which the analog input is sampled, excluding clock source jitter. It is the total jitter if the clock source is jitter free (ideal). Jitter diverges slowly as measurement time increases because of "1/f" noise, important at low frequencies (< 10 kHz). The specified jitter takes into account the white noise sources only (thermal and shot noise). For high-speed samplers this is reasonable, since even long data records span a time shorter than the time scale important for 1/f noise. For white-noise caused jitter, the clock and aperture jitter can be added in an rms manner to obtain the total sampling jitter.

If the underlying voltage noise mechanism of the sampling jitter has a white spectrum, the sampled signal will display a white noise floor as well. In this case, the required aperture jitter, Δt, to achieve a certain SNR, for a full-scale sinewave at frequency, f, is given by (B. Razavi, Principles of Data Conversion, IEEE Press, 1995, Appendix 2.1):

$$SNR\,(dB) = -20\log(2\pi f\Delta t)$$

If this TH is used in front of an n-bit ADC, then the ideal ADC SNDR is given by:

$$SNDR\,(dB) = 10\log(3/2) + 20\log(2)n = 1.76 + 6.02n$$

In order that the TH jitter performance do not limit the ADC performance, the jitter must fulfill:

$$\Delta t \le \frac{1}{\sqrt{6}\pi 2^n f}\ .$$

Note that this is independent of the sampling rate, so undersampling does not improve jitter tolerance. The averaging that is often combined with undersampling in test equipment, does improve jitter tolerance (and tolerance to other white noise effects).

The criterion above is sharper than the standard (incorrect) time-domain slope estimate by a factor √6. The reason is that n-bit quantization requires an rms error of (quantization step)/√12, which is considerably smaller than the quantization step error implicitly allowed in the usual time-domain estimates (another √2 comes from the energy of a sine wave relative to its amplitude squared).

The time-domain maximum slope argument can be appropriate for non-sinusoidal inputs, such as those encountered in instrumentation. If the rms error, ∆V, in the maximum slope region, slope FSR/(rise time), is used to define an effective number of bits, n, then the jitter simply needs to fulfill:

$$\Delta t \le \frac{rise\ time}{2^n}$$

Clock Jitter. The standard deviation of the mid-points of the relevant (rising or falling) edge of the clock source relative to the ideal edge (best fit). This jitter can be derived from the phase noise of the clock source, where the lower frequency bound of integration should correspond to the duration of a measurement record that the source will be used for.

Common-Mode Rejection Ratio (CMRR). Proportionality coefficient of the differential output and the common mode component of input signal. If an ideal symmetric input is available, CMR is the ratio of the differential output to the input on either input pin. A high-quality 50-ohm splitter may be used to generate the symmetrical inputs.

Full Scale Range (FSR). The maximum difference between the highest and lowest input levels for which various device performance specifications hold, unless otherwise noted.

Gain. Ratio of output signal magnitude to input signal magnitude. For sinewave inputs, it is the ratio of the amplitude of the first (main) harmonic output (HD1) to the amplitude of the input.

Input Bandwidth (BW, bw). The input frequency at which the gain for sinewave input is reduced by 3 dB (factor 1/√2) relative to its average value at low frequencies. The low frequency range is defined as the range including DC over which the gain stays essentially constant. The high frequency range is characterized by an increase in gain variation versus frequency, at least including the eventual monotonic decrease of the gain (“roll-off”). The input bandwidth tends to be input amplitude dependent. It is normally largest for very small inputs (small signal bandwidth, bw) and smallest for FSR inputs (large signal bandwidth, BW).

Settling Time (ts). The delay between the time that a track-and-hold circuit (TH) enters hold mode and the time that the TH hold capacitor nodes settle to within some specified precision. The settling time sets a lower limit on the required hold time during clocked operation.

Spectrum. The finite Fourier transform (FFT) of the discrete-time-sampled TH output. Ideally, this is obtained with a very high-resolution ADC quantizing the TH output with a clock rate locked to the TH clock (the ADC may be clocked at a slower rate than the TH). In the case of a dual TH (DTH), we can also use the beat frequency test, where the input frequency is close to an integer multiple of the clock frequency, and the DTH output is fed directly into a spectrum analyzer. The DTH output then contains little high frequency energy and the low frequency part of the spectrum analyzer sweep accurately represents the TH spectrum that would have been obtained with the ADC method.

Spurious Free Dynamic Range (SFDR). The ratio of the magnitude of the first (main) harmonic, HD1, and the highest other harmonic (or non-harmonic other tone, if present), as observed in the TH spectrum. The input is FSR, unless otherwise noted. SFDR in dB is given by 20log (SFDR as amplitude ratio), and is generally positive.

Total Harmonic Distortion (THD). The ratio of the square root of the sum of the harmonics 2 to 5 to the amplitude of the first (main) harmonic in the TH spectrum. THD in dB is given by 20log (THD as amplitude ratio), and is generally negative.

Theory of Operation

The DTH chip contains two TH’s, TH1 and TH2, in series, together with clock shaping circuitry, BUFFER1 and BUFFER2, and a 50-ohm output driver, OUTBUF (Figure 1). To maximize dynamic range and insensitivity to noise, all non-DC internal circuits and all non-DC inputs and outputs are differential. TH1 determines the dynamic sampled-mode performance of the DTH. Its sampling bridges exploit the ultra-high speed of the Schottky diodes available in the GaAs HBT process. TH1 clock inputs, CLK1P and CLK1N, should be driven by a low-jitter clock source. TH2 is similar to TH1, except that its bandwidth requirement is lower and its gain is closer to unity.

The DTH receives a differential analog input signal at inputs INP and INN, which is sampled on the TH1 hold capacitors upon a falling transition of its differential clock voltage V(CLK1P) – V(CLK1N), after an aperture delay, ta, see Figure 3. TH1’s aperture delay is positive, nominally 60ps.

The sampling instant is affected by clock source jitter (off-chip) and aperture jitter (caused by on-chip noise). From the Definition of Terms, the required total sampling jitter for sampling a 1 GHz 1 Vpp sine wave with 10-bit accuracy is 127 fs. The aperture jitter of the RTH040 is less than 100 fs for a 1 GHz 0.5 Vpp TH1 clock, CLK1. Using RMS addition of jitter, the clock source jitter must be less than 80 fs (over the measurement record time) for direct 10-bit sampling of GHz range signals. Given a noise variance, ΔV, of the on-chip clock buffer, its aperture jitter, Δt, is inversely proportional to the clock buffer gain and the slew rate of the incoming clock at the zero-crossing point:

$$\Delta t = \frac{\Delta V}{gain \times slew\, rate}\ .$$

For low slew rates or frequencies, the clock buffer gain is constant and its aperture jitter is inversely proportional to the input clock slew rate, improving with increasing slew rate. For high slew rates or high frequencies, the jitter increases again, because the buffer gain drops steeply. For the RTH040, the clock buffer gain is still roughly constant up to 1 GHz, so that the aperture jitter is inversely proportional with the slew rate of the incoming clock. In the above equation, we have $\Delta V/gain$ ≈ 0.15 mV. The RTH040 aperture jitter at various slew rates can then be estimated. For example, a 1 GHz 0.5 Vpp sinusoidal CLK1 signal corresponds to a slew rate ~ 1.6 V/ns, correctly yielding an aperture jitter < 100 fs.

The held and buffered output of TH1, VTH1, is sampled on the TH2 hold capacitors upon a falling transition of its differential clock voltage V(CLK2P) – V(CLK2N), after an aperture delay closely equal to that of TH1. This allows simple out-of-phase clocking of TH1 and TH2 by having opposite phases for CLK1 and CLK2. Aperture jitter of TH2 is irrelevant, since the slew rate of the TH2 input is equal to the TH1 differential droop rate, about 1000x lower than the input slew rate for TH1 for a 1 GHz 1 Vpp sine wave. TH2 can be in track mode before TH1 switches to hold, but a minimum track time of TH2 after TH1 enters hold mode must be observed to ensure that TH2 has fully acquired the TH1 output (ttrack2, min).

Hold mode feedthrough, or in to out hold-mode gain in dB, again is important for TH1 and not for TH2, since any distortion on the held TH1 signal by a rapidly varying TH1 input will be sampled by TH2, and can not be removed. RTH040's TH1 hold mode feedthrough performance is more than sufficient for 10 bit sampling of GHz range signals.

After a TH1 postamplifier, TH2 produces an output VTH2. For out-of-phase clocking, the delay from the hold instant of TH1 to the ideal sampling time of circuitry after TH2 is close to one full clock cycle, for example 1 ns at a 1 GHz sampling rate. The TH2 output is flat for more than half a clock cycle, which eases the bandwidth requirement of subsequent circuitry. This is true, even though a small glitch will be present at the transition from track to hold of TH2 and the output is only 10 bit accurate during the latter part of half a clock cycle.

Lower limits for the sampling rates of TH1 and TH2 are set by single-ended hold-mode droop rates, and lead to the specification of maximum hold times (thold1, max and thold2, max). For longer hold times, the DTH must be allowed sufficient recovery time during track phase (or a sequence of track phases), so it can return to normal operation mode. The bandwidth of subsequent circuitry can be minimal if TH2 is clocked at its lowest recommended frequency, 10 MHz. Since TH1 should be clocked at least at 100 MHz, and possibly faster to meet jitter requirements, CLK1 and CLK2 can be chosen different, as long as they are locked to each other with a proper phase relationship. Minimum required single-pole bandwidth at the output for 10-bit precision is $(10\ln2/2\pi)$ x f_{CLK2}, or approximately $1.1f_{CLK2}$. In practice, <20 MHz bandwidth of subsequent circuitry would be sufficient, if f_{CLK2} is 10 MHz.

One digital input, Track Mode Select (TMS), is provided to put both TH's in track mode, independent of the clock signals. The bandwidth of the DTH is substantially lower in this mode than in the sampled mode. The TMS is useful for low sample-rate operation, including DC testing.

Signal Descriptions

The RTH040 inputs are terminated on-chip with 50 Ω to GND. This automatically protects against off-chip high-impedance high-voltage disturbances. The absolute maximum rated voltage at input termination resistors is ±1 V, at 20 mA current. The RTH040 is designed for 1 Vpp differential input signals, and can accept common-mode offsets up to ±100 mV. If operated in single-ended mode, terminate the complementary input off-chip with 50 Ω to the same common mode as the driven input. The single-ended FSR is half that of the differential FSR. Distortion in the single-ended mode can be up to 6 dB higher than in differential mode, and differential input should be used for optimal performance. The INP and INN inputs are equivalent, except for the polarity of their effect on OUTP and OUTN.

All four clock input signals are terminated on-chip with 50 Ω to GND. Use differential clock signals for optimal performance. Large CLK1 edge rate benefits aperture jitter performance, small CLK1 and CLK2 amplitudes minimizes distortion due to clock feed-through in the higher clock frequency range (500 to 1000 MHz). In case of single-ended clocking the complementary input(s) can be terminated directly to GND (lowest noise, clock waveform distortion is not critical). Distortion for single-ended clocks can be several dB higher than for differential clocks, and differential clocks should be used for optimal performance.

The track-mode select, TMS, can simply be left open for the (default) sampled-mode operation of the RTH040. Grounding the TMS puts both track-and-holds, TH1 and TH2, in track-mode. In this state, the TMS draws up to 0.75 mA of current.

Due to its highly differential design, the RTH040 requires relatively modest power supply decoupling. The 0.01 μF capacitors VEE to GND and VEE to VCC (Figure 4) should be placed as close to the package as possible. Larger low frequency power supply decoupling capacitors, VEE to GND and VCC to GND, should be placed within 1 inch of the RTH040. Depending on the expected noise on the supplies more capacitors in parallel may need to be used. With low-impedance supplies that are very quiet (no digital circuitry), the RTH040 can also perform well with no external decoupling at all.

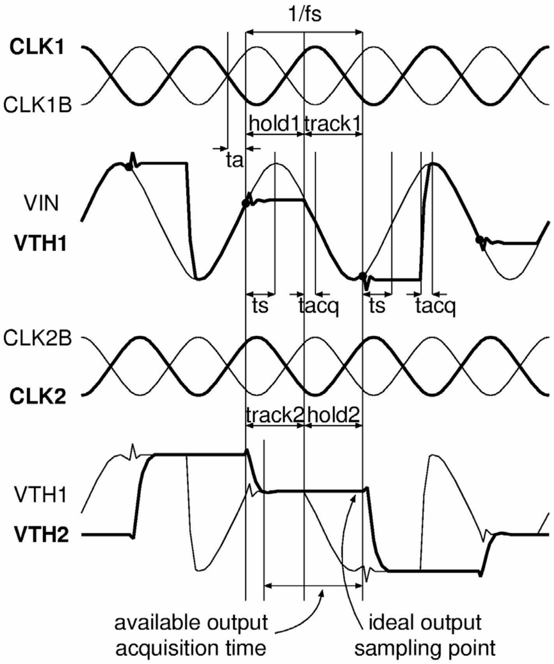

Figure 3. Timing diagram for out-of-phase clocking of TH1 and TH2

Typical Operating Circuit

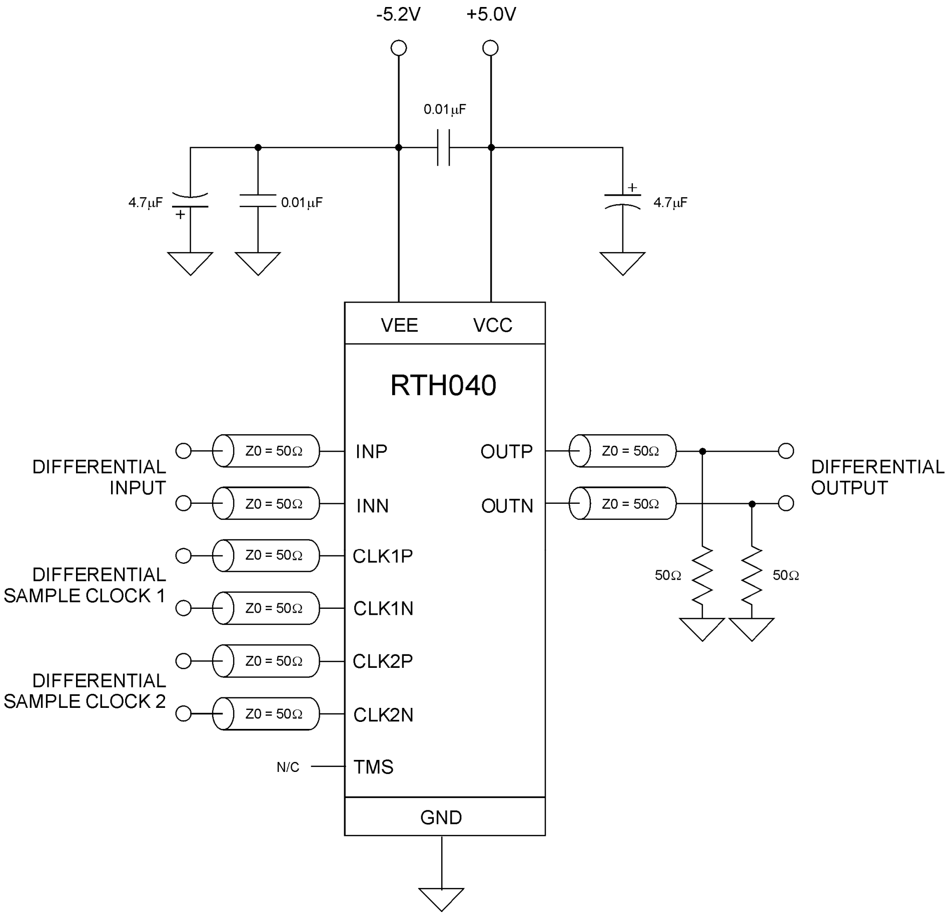

**Figure 4. Typical interface circuit (sampled mode, connect TMS to GND for track mode)
All differential inputs are terminated on-chip with 50 Ω to GND.**

Typical Performance

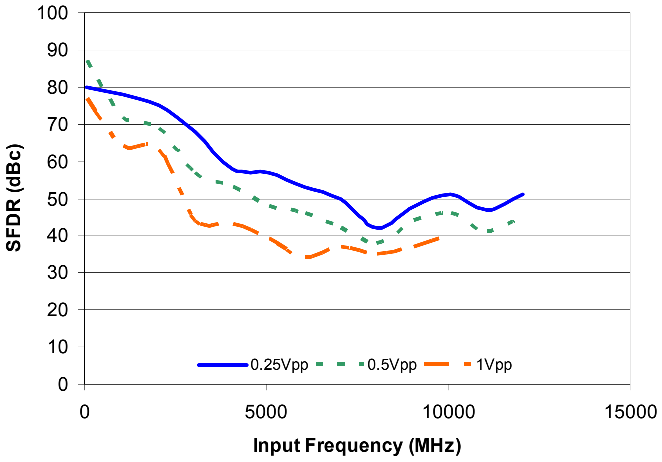

Figure 5. SFDR x Fin, single tone.

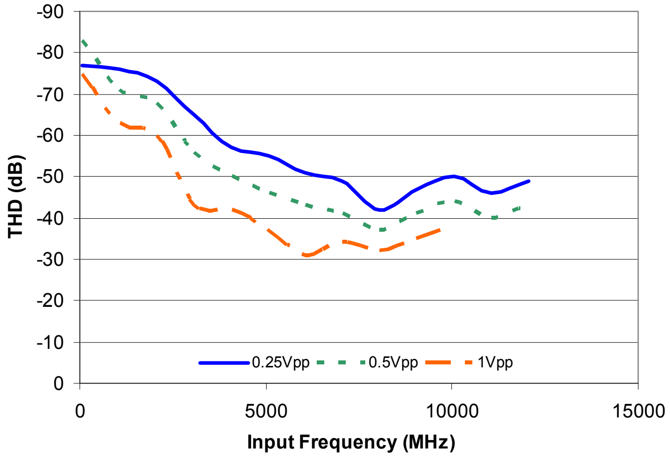

Figure 6. THD x Fin, single tone.

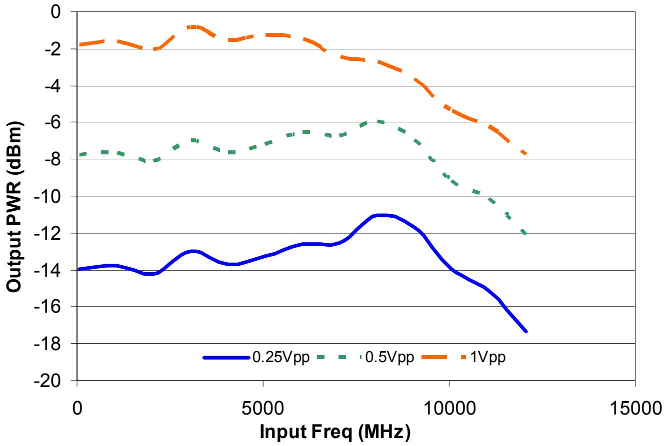

Figure 7. Input bandwidth.

Die Plot and Pad Arrangement

The inputs and output of the RTH040 are arranged in a ground-signal-ground-signal-ground (GSGSG) configuration on opposite sides of the die. The clock signals come in under an orthogonal direction, which reduces inductive coupling to the signal path, both for bond wires and for package leads. The part does not require other components inside the package, since sufficient bypass capacitance is supplied on-chip.

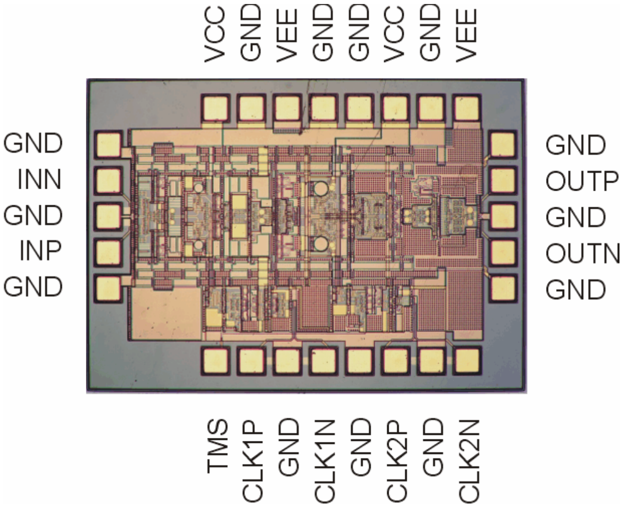

Figure 8. RTH040 die photo and pad arrangement; Die size: 75 x 55 x 7 mils (1.899 x 1.375 x 0.178 mm); Pad pitch: 5.91 mil (0.150 mm); Die photograph for pad placement reference only.

Package Information

The package is a 24 lead metallized ceramic base glass sidewall Quad Flat Pack (QFP). The leads are trimmed to 0.150 inch (3.81mm) length. The thermal impedance (junction to base) is approximately 15 °C/W. The lid is sealed with epoxy.

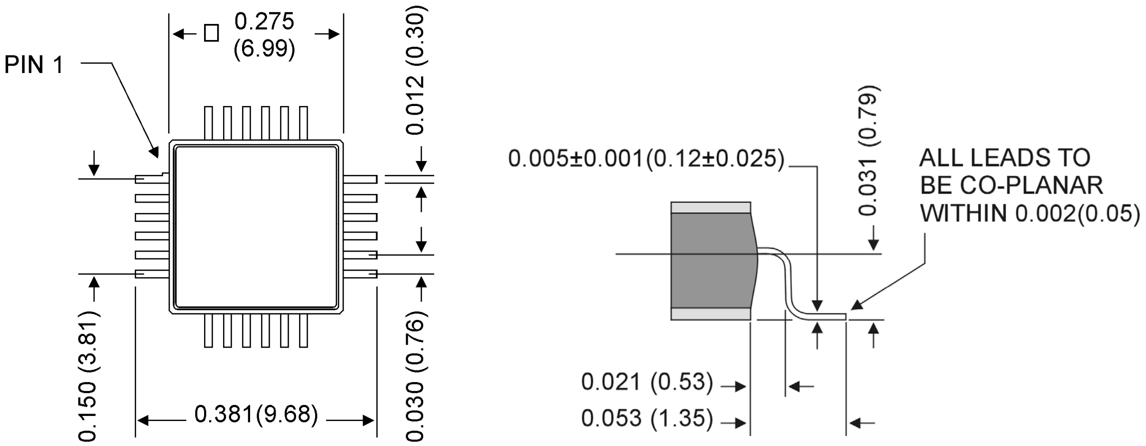

Figure 9. RTH040-QP package outline, dimensions in inches (mm), tolerance ±0.002” (±0.051mm).

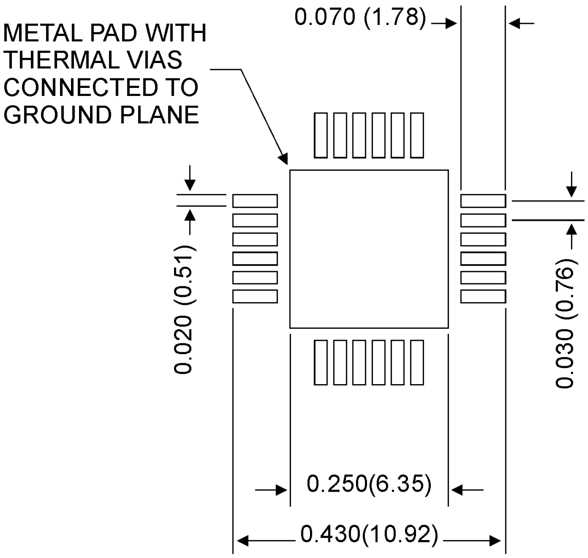

Figure 10. RTH040-QP footprint, dimensions shown in inches (mm).