TELEDYNE
SCIENTIFIC COMPANY

RDS010

900MHz Direct Digital Frequency Synthesizer (DDFS)

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RDS010

900MHz Direct Digital Frequency Synthesizer (DDFS)

Features

- 900MHz Clock Frequency
- 0 to 450MHz Tuning Bandwidth
- 32Bit Frequency Resolution
- Dual Frequency Control Register
- 12Bit Phase Modulation
- Dual Phase Control Register
- Latency of 23 Clock Cycles
- Integrated 12Bit DAC
- 60dBc SFDR
- 0dBm Output Power
- 3.3V Power Supply
- 3.5W Power Dissipation
- CMOS compatible Data Inputs
- Internally Terminated Outputs
- 88 Pin QFP Hermetic Ceramic Package

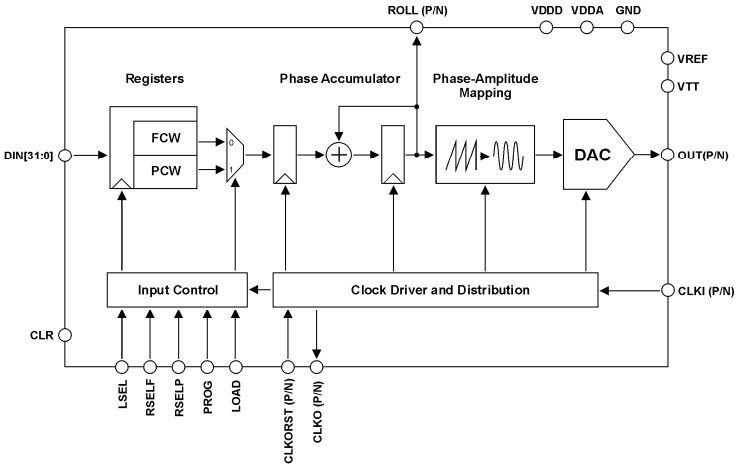

Figure 1 - Functional Block Diagram

Product Description

The RDS010 is a high performance SiGe direct digital frequency synthesizer (DDS) with a clock frequency of 900MHz. The RDS010 has been optimized for ultra-high speed applications, achieving better than 60dBc of spurious output at 900MHz reference clock frequency. On-chip DAC outputs are internally terminated with 50Ω resistors for better dynamic performance.

Ordering information

PART NUMBER	DESCRIPTION
RDS010-QP	900MHz DDFS, QFP Package
RDS010-DI	900MHz 32Bit FCW DDFS, DIE
EVRDS010-QP	RDS010-QP Evaluation Board

CAUTION
DEVICE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)

Absolute Maximum Ratings

Supply Voltages

Between GNDs ..... -0.3 to +0.3 V
Between VDDs ..... -0.3 to +0.3 V
VDDs to GND ..... -1 V to +4 V

RF Input Voltages

CLKIP, CLKIN to GND ..... -1 to +4 V
CLKORSTP, CLKORSTN to GND..... -1 to +4 V

DC Analog Input Voltages

VTT to GND V

Digital Input Voltages

CLR to GND V
DI<31:0> to GND V
LSEL to GND V
RSELF, RSELP to GND V
PROG to GND V
LOAD to GND V

Output Termination Voltages

OUTP, OUTN to GND V
CLKOP, CLKON to GND V
ROLLP, ROLLN to GND V

Temperature

Case Temperature..... -15 to +85 °C
Junction Temperature..... +100 °C
Lead, Soldering (10 Seconds) ..... +220 °C
Storage..... -40 to 125 °C

DC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VDD = 3.3V; VREF = 1.3V; VTT = 1.3V; Clock: 900MHz, 0.6Vpp Differential; Outputs Terminated Into 50 Ω to VDD.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
1.0	**TEMPERATURE DRIFT**						
1.1	Warm-up Time		After Power-up			30	s
2.0	**CLOCK INPUT (CLKIP, CLKIN)**						
2.1	Input Resistance	R_{CLKI}	Resistance (CLKI P/N) to VTT	45	50	55	Ω
2.2	Input Capacitance	C_{CLKI}			1.5		pF
3.0	**HIGH SPEED DIGITAL INPUT (CLKORSTP, CLKORSTN)**						
3.1	Input Resistance	R_{HDIN}	Resistance to VTT		50		Ω
3.2	Input Capacitance	C_{HDIN}			1.5		pF
4.0	**DIGITAL INPUTS (DI<0:31>, CLR, EN, PROG, LSEL, RSELF, RSELP, LOAD)**						
4.1	Input Capacitance	C_{DIN}			1.5		pF
5.0	**ANALOG OUTPUTS (OUTP, OUTN)**						
5.1	Output Voltage Swing	V_{FSD}	Differential, Terminated Into 50Ω to VCC=3.3V on Each Output		630		mVpp
5.2	Output Voltage Swing	V_{FSS}	Single Ended, Terminated Into 50Ω to VCC=3.3V		315		mVpp
5.3	Output Voltage Range	V_{FSRS}	Single Ended, Terminated Into 50Ω to VCC=3.3V (MIN=000h, MAX=FFFh)	2.9		3.3	V
5.4	Output Current	I_{OUT}	Terminated Into 50Ω to VCC=3.3V		6		mA
6.0	**CLOCK OUTPUT (CLKOP, CLKON)**						
6.1	Common Mode	$V_{CM,CKO}$	Differential LVPECL		2		V
6.2	Differential Voltage	$V_{DF,CKO}$	Differential LVPECL	200		800	mV
7.0	**DIGITAL OUTPUT (ROLLP, ROLLN)**						
7.1	Common Mode	$V_{CM,RR}$	Differential LVPECL		2		V
7.2	Differential Voltage	$V_{DF,RR}$	Differential LVPECL	200		800	mV
8.0	**REFERENCE (VREF)**						
8.1	Input Resistance	R_{VREF}					Ω
9.0	**POWER SUPPLY REQUIREMENTS**						
9.1	Positive Current, Analog	IDDA					mA
9.2	Positive Current, Digital	IDDD					mA
9.3	Power Dissipation	P			3.5		W

AC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VDD = 3.3V; VREF = 1.3V; VTT = 1.3V; Clock: 900MHz, 0.6Vpp Differential; Outputs Terminated Into 50 Ω to VDD.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
10.0	**DYNAMIC PERFORMANCE**						
10.1	Spurious Free Dynamic Range	SFDR1	F_{clk} = 900MHz , F_{out} = 56MHz		72		dBc
10.2		SFDR2	F_{clk} = 900MHz , F_{out} = 225MHz		65		dBc
10.3		SFDR3	F_{clk} = 900MHz , F_{out} = 300MHz		62		dBc
10.4	Clock Feedthrough	FD	Spurs at F_{clk} = 900MHz				dBc
10.5	Output Flatness	ATT	Attenuation at F_{out} = 400MHz				dB
10.6	Phase Noise	PN1	F_{out} = 250MHz, 1kHz Offset		-140		dBc/Hz
10.7		PN2	F_{out} = 250MHz, 10kHz Offset		-150		dBc/Hz
10.8		PN3	F_{out} = 250MHz, 100kHz Offset		-152		dBc/Hz

Operating Conditions

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
11.0	**CLOCK INPUTS (CLKIP, CLKIN)**						
11.1	Amplitude	$V_{DF,CLKI}$	Differential LVPECL or Sinusoidal	200		800	mV
11.2	Common Mode Voltage	$V_{CM,CLKI}$	Differential LVPECL or Sinusoidal	1.5	2	3	V
11.3	Maximum Frequency	$F_{MAX,CLKI}$		900			MHz
11.4	Minimum Frequency	$F_{MIN,CLKI}$				1	MHz
12.0	**HIGH SPEED DIGITAL INPUT (CLKORSTP, CLKORSTN)**						
12.1	Amplitude	$V_{DF,CKOR}$	Differential LVPECL	200		800	mV
12.2	Common Mode Voltage	$V_{CM,CKOR}$	Differential LVPECL	1.7	2	2.8	V
13.0	**DIGITAL INPUTS (DI<0:31>, CLR, EN, PROG, LSEL, RSELF, RSELP, LOAD)**						
131	Input High Voltage	$V_{IH,DIN}$		1.7			V
13.2	Input Low Voltage	$V_{IL,DIN}$				1.2	V
14.0	**TIMMING CHARACTERISTICS**						
14.1	DIN to PROG Setup	t_{STDTPG}		400			ps
14.2	DIN to PROG Hold	t_{HDDTPG}		250			ps
14.3	RSEL, LSEL to PROG Setup	t_{STCTPG}		350			ps
14.4	RSEL, LSEL to PROG Hold	t_{HDCTPG}		400			ps
14.5	LOAD to CLKO Setup	t_{STLDCK}		700			ps
14.6	LOAD to CLKO Hold	t_{HDLDCK}		0			ps
14.7	RSEL, LSEL to LOAD Setup	t_{STCTLD}		210			ps
14.8	RSEL, LSEL to LOAD Hold	t_{HDCTLD}		150			ps
14.9	CLKORST to CLKI Setup	t_{STCRCK}		50			ps
14.10	CLKORST to CLKI Hold	t_{HDCRCK}		400			ps
14.11	Load to Output Latency	LTC		23		23	CLKI
15.0	**TERMINATION VOLTAGE (VTT)**						
15.1	Reference Voltage	V_{TT}	Termination Voltage for CLKI		1.3		V
16.0	**REFERENCE (VREF)**						
16.1	Reference Voltage	V_{REF}			1.3		V
17.0	**POWER SUPPLY REQUIREMENTS**						
17.1	Supply Voltage, Analog	VDDA		3.1	3.3	3.5	V
17.2	Supply Voltage, Digital	VDDD		3.1	3.3	3.5	V
18.0	**OPERATING TEMPERATURE**						
18.1	Case Temperature	Tc	Measured at Bottom Plate	-15		85	°C
18.2	Junction Temperature	Tj				120	°C

Pin Description

P/I/O	PIN	NUM.	NAME	FUNCTION
P	1, 2, 6, 7, 52, 54, 55	7	VDD	Digital VDD Power Supply
P	71, 72, 73, 74, 75	5	VDDA	Analog VDD Power Supply
P	58, 59, 60, 61, 62, 63, 64, 68, 69, 70, 77, 78, 79, 84, 85, 86, 87, 88, bottom plate	18	GND	Ground
I	4	1	VTT	Input Clock Termination Voltage
I	76	1	VREF	DAC Core Reference Voltage
I	16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 31, 32, 33, 34, 35, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51	32	DI<0:31>	DI<0:31> is the 32Bit input Data. MSB is Bit 31 FCW uses DI<0:31>, PCW uses DI<0:11>
I	13	1	LSEL	Frequency / Phase Selection: 0 - Frequency 1 - Phase
I	14	1	RSELF	Frequency Register Selection: 0 - Register 1 1 - Register 2
I	15	1	RSELP	Phase Register Selection: 0 - Register 1 1 - Register 2
I	30	1	PROG	Program Control Signal. Active High
I	36	1	LOAD	Load The NCO Accumulator. Synchronous with CLKO
I	10	1	CLR	NCO Clear Signal. Active High
I	9	1	CLKORSTP	High Speed Output Clock Reset
I	8	1	CLKORSTN	
I	5	1	CLKIP	CLKIP / CLKIN Is Differential Input Clock
I	3	1	CLKIN	
I	53	1	EN	Device Enable: 0 - Disable 1 - Enable
O	11	1	ROLLP	ROLLP / ROLLN Is Differential NCO Accumulator Overflow
O	12	1	ROLLN	
O	38	1	CLKOP	CLKOP / CLKON Is Differential Output Clock (Operating Clock Divided by 4)
O	37	1	CLKON	
O	66	1	OUTP	OUTP / OUTN Is Differential Output
O	65	1	OUTN	
RES	82	1	RESP	Reserved – connect to VDD
RES	80, 81, 83	3	RESN	Reserved – connect to GND
RES	56, 57, 67	3	RES	Reserved – No connect

All digital inputs are CMOS compatible, except: CLKi(P/N) and CLKORST(P/N), which are LVPECL. The outputs CLKO(P/N) and ROLL(P/N) are also LVPECL.

Pin Layout (TOP view)

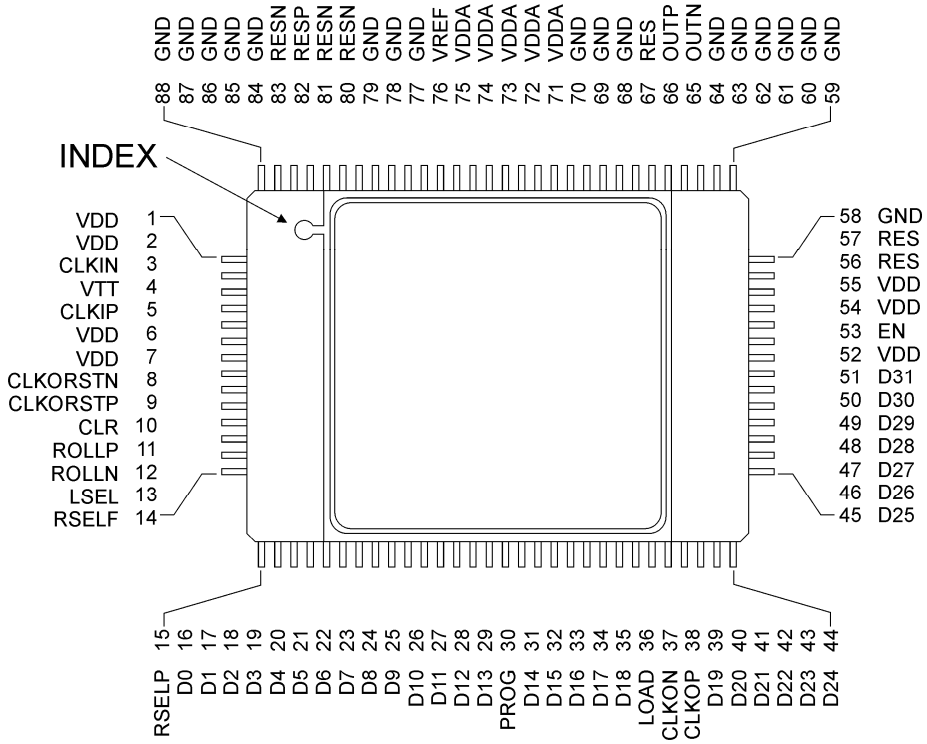

Figure 2 - RDS010-QP pinout (top view).

Theory of Operation

The RDS010 is a single chip direct digital frequency synthesizer with a numerically controlled oscillator (NCO) and a digital to analog converter (DAC). The NCO can be divided into three blocks: input, accumulator and phase to amplitude mapping. The input interfaces the NCO with the exterior. It controls the programming, frequency and phase, of the DDFS. After a new frequency or phase is programmed, the accumulator generates a ramp that sweeps through the full range of possible phase values with the desired frequency. Those values address the phase to amplitude mapping to determine a digitized sine amplitude value. The DAC is then employed to convert the digital data to an analog waveform.

The DAC employs 4Bit segmentation and 8Bit binary-weighted codes for high-speed and best dynamic performance. The 12Bit NCO output is latched by master-slave flip-flops immediately after the buffers to reduce the data skew. The 4 MSB data bits are decoded into thermometer code by a two-stage decoding block, and the 8 LSB data bits are transported through the delay equalizer block. The digital data are then synchronized again by a second master-slave flip-flop to reduce the switching glitch. The decoded 4 MSB data drive 15 identical current switches, and the 8 LSB data drive 8 current switches. The output nodes from the LSB current switches are connected to the analog output through an R-2R ladder to generate the binary output. The DAC of RDS010 provides output terminated at 50Ω. For static linearity performance, randomized current source resistors and switching sequence are implemented. VREF pin can be used to override the internal reference with an accurate, temperature-compensated external voltage reference.

Programming the RDS010

Programming the RDS010 is done in two steps. The first step writes the 32bit input data to the selected control register. The second step loads the contents of the selected control register into the accumulator. During the first step the, which is asynchronous, the control register to be written is selected using LSEL (frequency or phase control register) and RSELF/RSELP, which select the register 0 or 1. The input data is then written to the select register during the rising edge of PROG. The second step is synchronous with the operating clock and is done by sampling LOAD with CLKO. LSEL is used to indicate if a frequency or phase control word is going to be loaded into the accumulator. When loading a new frequency control word (FCW) into the accumulator, RSELF indicate which frequency control register contains the desired FCW. RSELP can assume any state. In the case a new phase control word (PCW) is going to be loaded, RSELP indicate which register to use and RSELF should indicate which frequency control register contains the current FCW being used in the accumulator.

Timming Diagrams

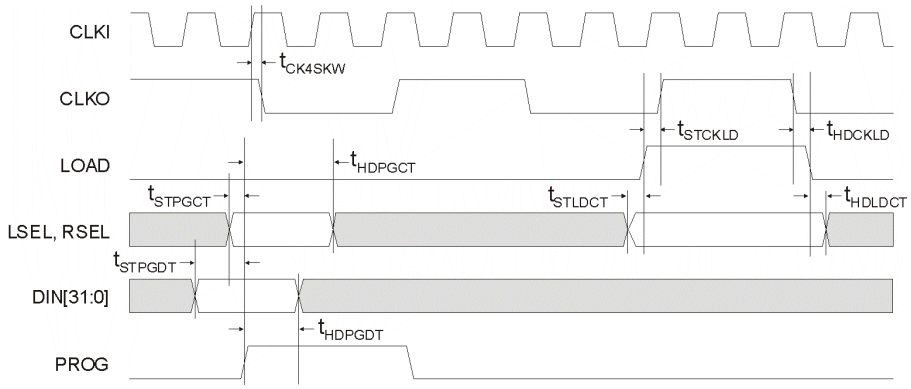

Figure 3 - Input register programming and NCO load

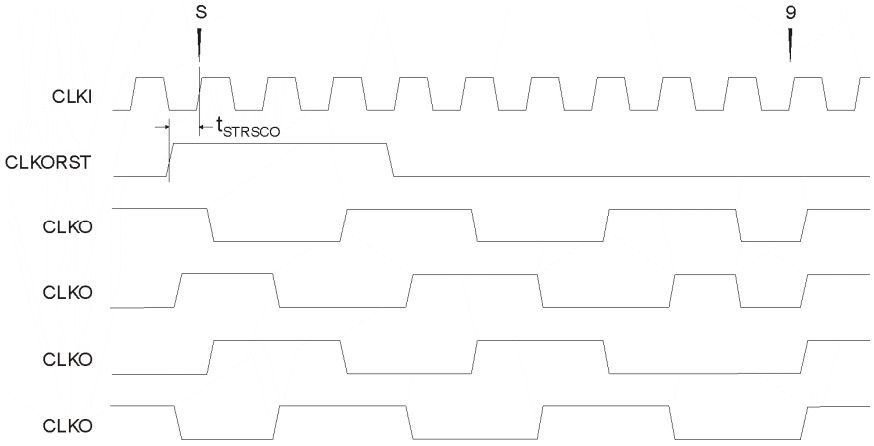

Figure 4 – Output clock reset

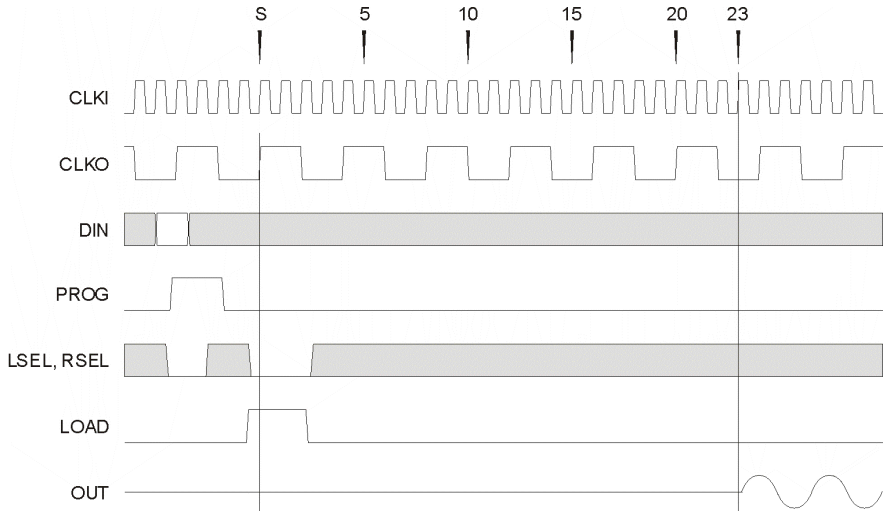

Figure 5 - Latency

Typical Operating Circuit

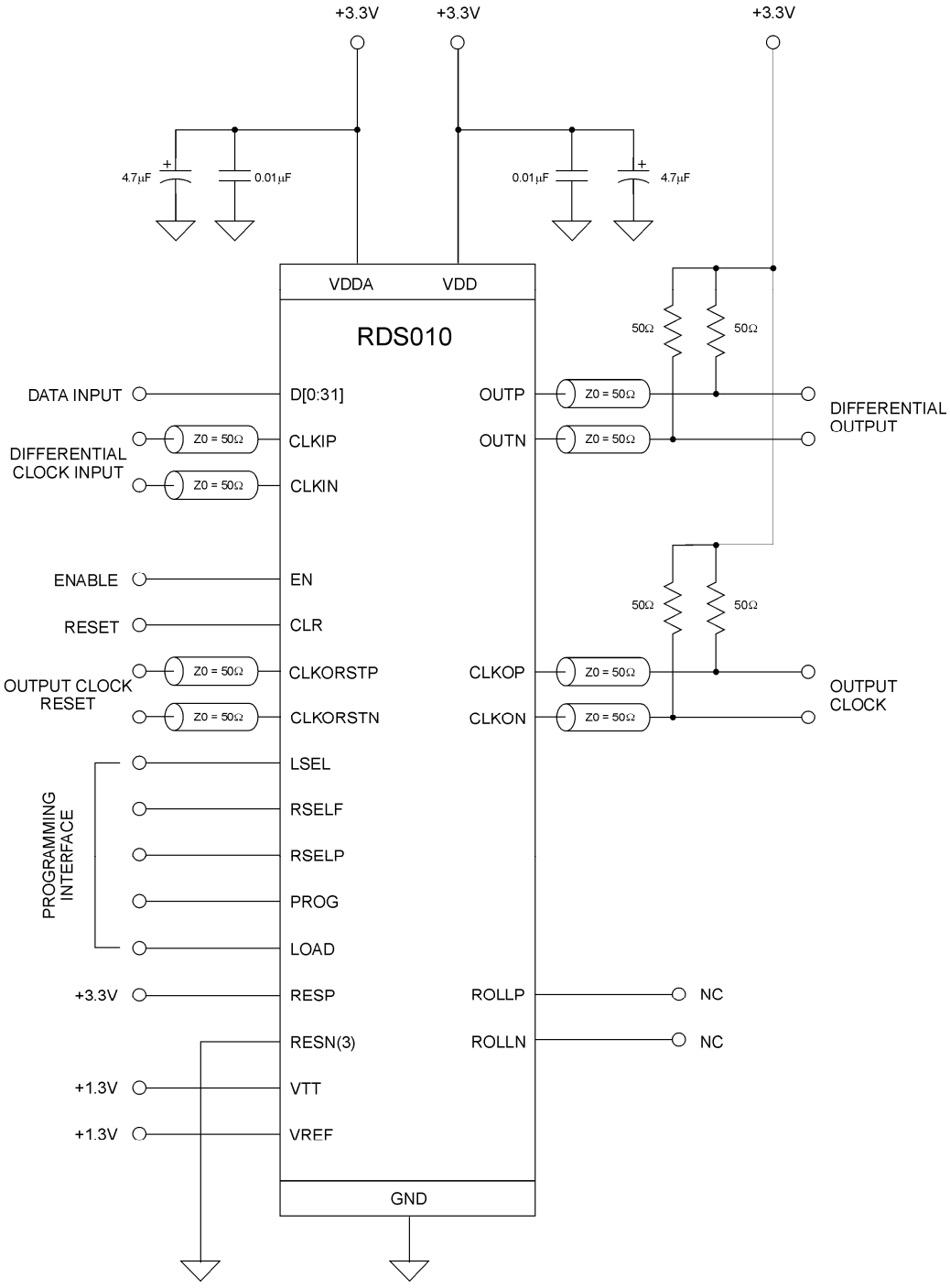

Figure 6 - RDS010-QP typical operating circuit.

Typical Performance

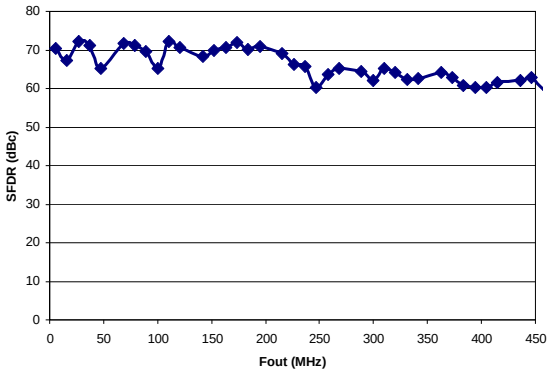

Figure 7 - SFDR x Fout with Fclk=900MHz

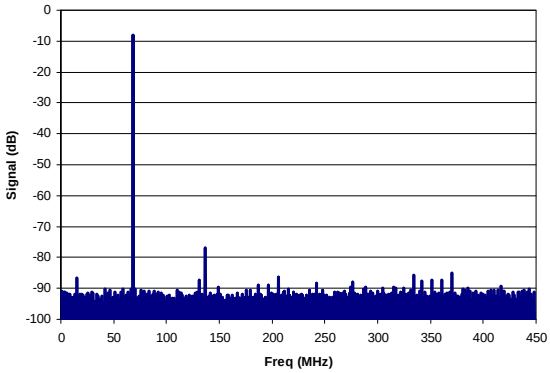

Figure 8 – Spectrum with Fclk=900MHz, Fout=68MHz

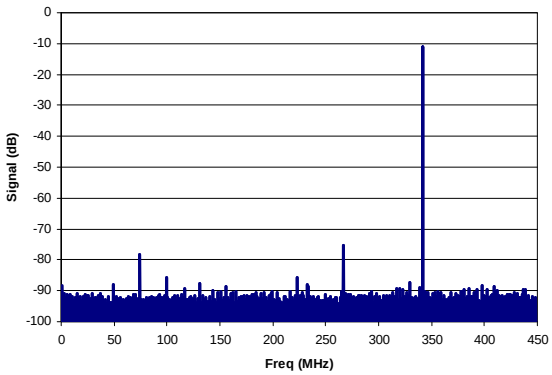

Figure 9 – Spectrum with Fclk=900MHz, Fout=341MHz

Package Information

The package is a 88 lead ceramic Quad Flat Pack (QFP) with a heat sink slug on the package's bottom. The leads are trimmed to 0.045 inch (1.15mm) length (from the package edge). The thermal impedance (junction to base) is approximately 3.5 °C/W.

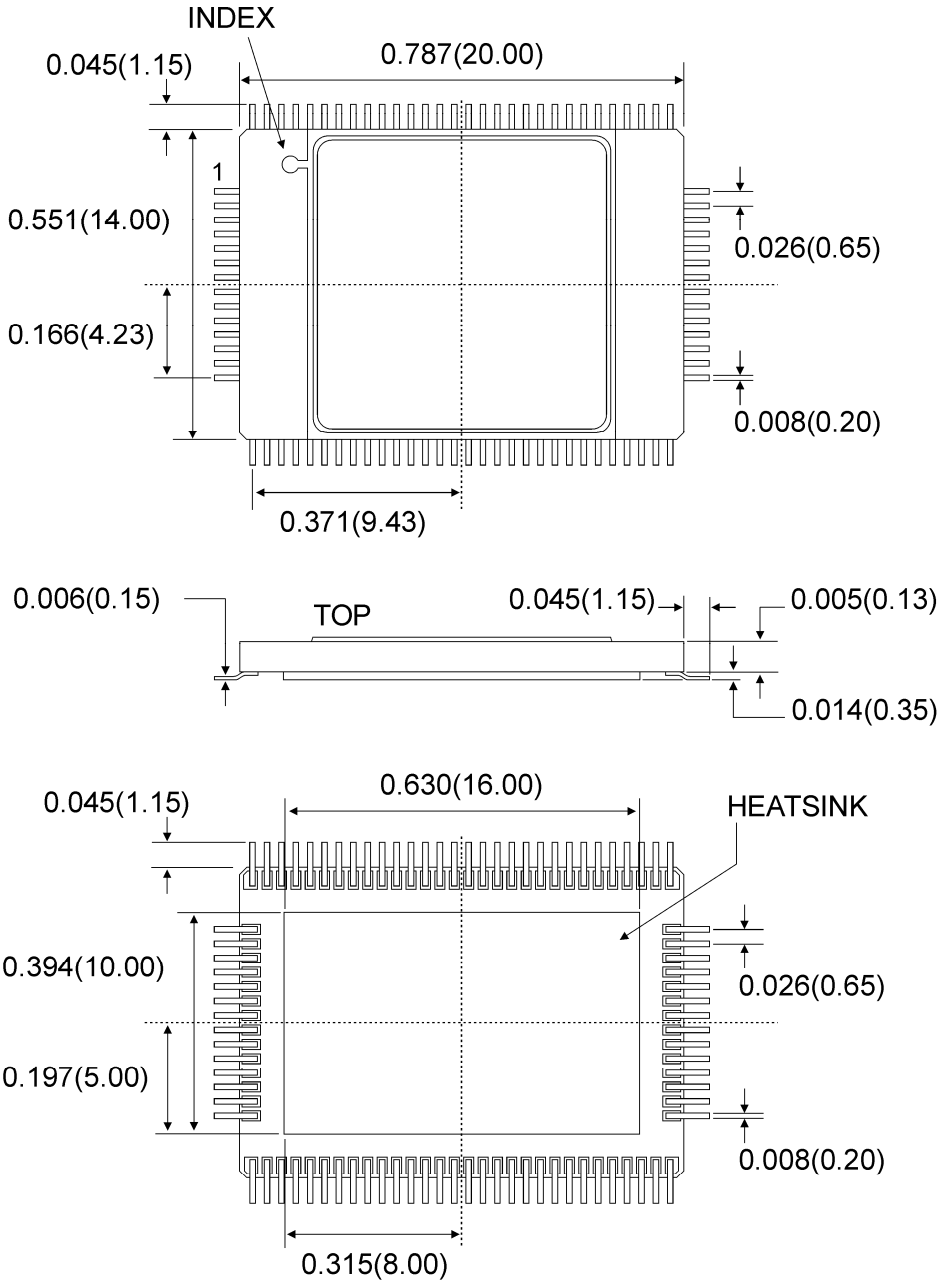

Figure 10 - RDS010-QP package, dimensions shown in inches (mm).