EVRTH070

Track and Hold Evaluation Module

Features

- SMA connectors for all signal / clock inputs and signal output.
- Fully Assembled and Tested.

Product Description

The EVRTH70 is an evaluation Module designed to demonstrate the performance of the Teledyne Scientific RTH070-HQ. The module comes fully assembled and tested, providing an easy way to evaluate the track and hold performance. All is needed are power, differential input and clock signals.

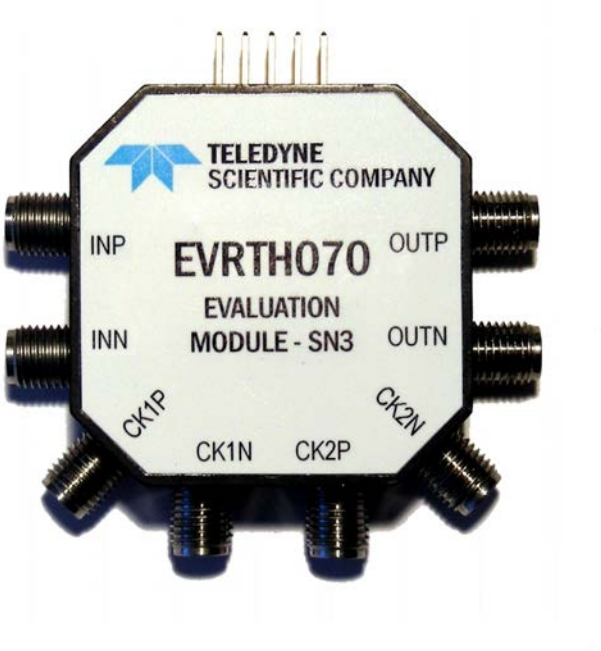

Figure 1– EVRTH70 Module

Ordering information

PART NUMBER	DESCRIPTION
EVRTH070	Track and Hold Evaluation Module with a RTH070-HQ

Signal Description

P/I/O	PIN	NUM.	NAME	FUNCTION
P	1,3,5	3	GND	Power Supply Ground
P	2,4,6,7,8,9	6	VEE	Negative Power Supply
I	SMA	1	CLK1P	Clock 1 Input: High = TH1 in Track Mode
I	SMA	1	CLK1N	Low = TH1 in Hold Mode
I	SMA	1	CLK2P	Clock 2 Input: High = TH2 in Track Mode
I	SMA	1	CLK2N	Low = TH2 in Hold Mode
I	K	1	INP	Analog Input
I	K	1	INN	
O	SMA	1	OUTP	Analog Output
O	SMA	1	OUTN	
R	10	1	NC	Reserved

Power Supplies

The evaluation module requires a negative supply voltage. VEE is a –5.4V supply (280mA nominal). The evaluation module also requires a ground connection. These connections are made using cables connected to the 5x2pin power header located at the side of the module (Fig 5).

Inputs

The EVRTH070 evaluation board has high performance, SMA connectors for the differential clocks and output signal. The input uses K connector. The clock and signal inputs are terminated on-chip with a 50Ω resistor to ground.

The input is self biased and if a DC connection is used the input common mode voltage should be observed (refer to the RTH070 datasheet).

The clocks CLK1P, CLK1N, CLK2P and CLK2N are the clocks for the two individual track and hold. The two track and hold can be clocked independently (as long as the phase relationship is maintained). Single ended or differential clock schemes can be used, although better dynamic performance is achieved with a differential clock. Figure 2 and Figure 3 illustrates simple out of phase clocking schemes, both differential and single ended. In the case of single ended clocking, the balun provide the CLK1P and CLK2P and the complementary inputs should be terminated with a 50Ω resistance to ground for optimum performance. Another option for a single ended configuration is to use a 180 degree power splitter instead of the balun. It is possible however to operate the evaluation board with single ended clocking by connecting the complementary clock inputs directly to ground, or even leaving them open (they are terminated on chip with a 50Ω resistor to ground, providing a sufficiently low impedance path to ground).

Outputs

The EVRTH070 has complementary voltage outputs, OUTP and OUTN, accessible through high performance SMA connectors. Both outputs should be terminated with a 50Ω resistance to ground. For single ended applications an output balun may be used.

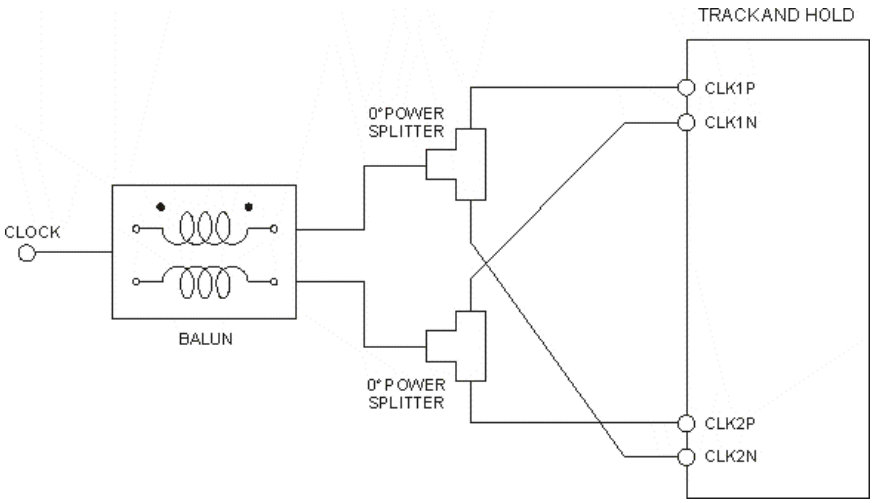

Figure 2– Setup for simple out of phase differential clocking

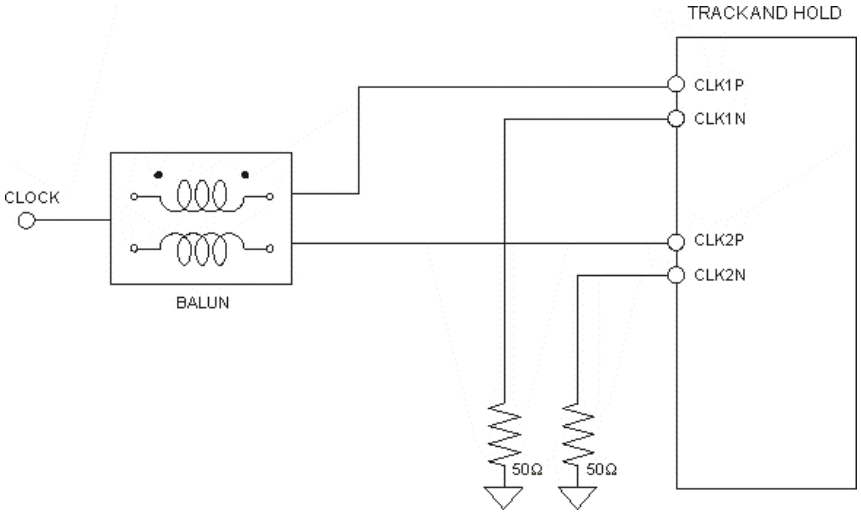

Figure 3– Setup for single ended clocking

Module Configuration

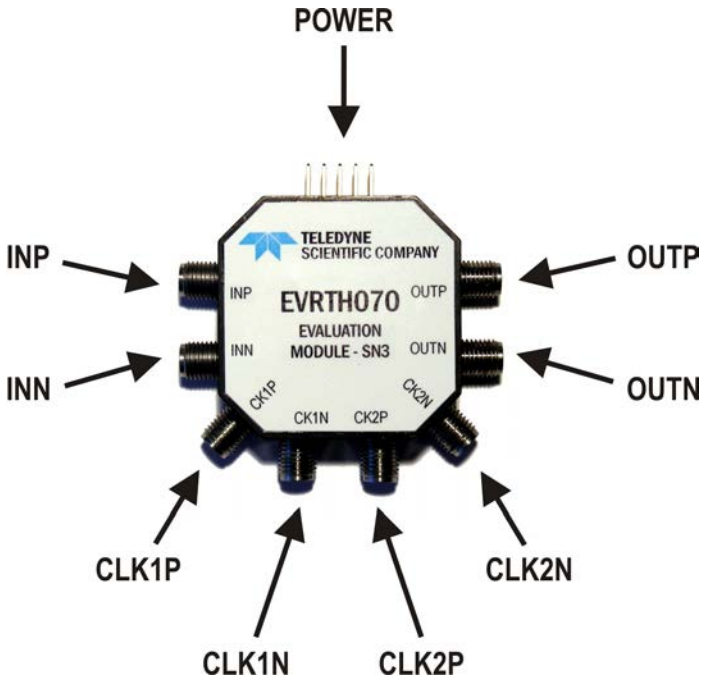

Figure 4 – Top view

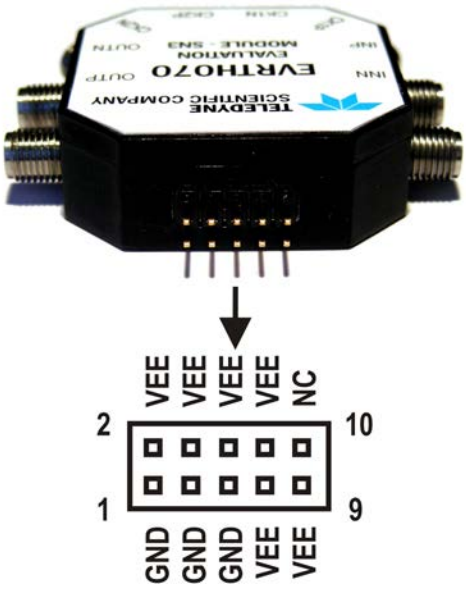

Figure 5 – Side view showing the power connector

Figure 6 – Side view showing the input, K connectors

Figure 7 – Side view showing the output, SMA connectors