TELEDYNE
SCIENTIFIC COMPANY

RAD004

6 Bit 4 GS/s Analog to Digital Converter

REV-DATE PC1-2412

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RAD004

6 Bit 4 GS/s Analog to Digital Converter

Features

- 6-Bit Resolution
- Up to 4 GS/s Sampling Rate
- Integrated Dual Track and Hold
- 0.5 Vpp Differential Full Scale Range
- 6 GHz Full Power Bandwidth (min)
- DNL: 0.5 LSB
- INL: 1 LSB
- ENOB: 4.5 Typical (DC to 4 GHz)
- No Missing Codes
- LVDS Compatible, Adjustable CML Output
- Grey Code Output
- Over-Range Indicator Output
- Integrated Pseudo Random Pattern Generator
- 2 Clock Cycles Latency
- 88 Pin QFP Package
- 7.5 W Power Dissipation
- 1 to 4 Demultiplexed Binary Output when Coupled with RDX004M4
- Lead Free

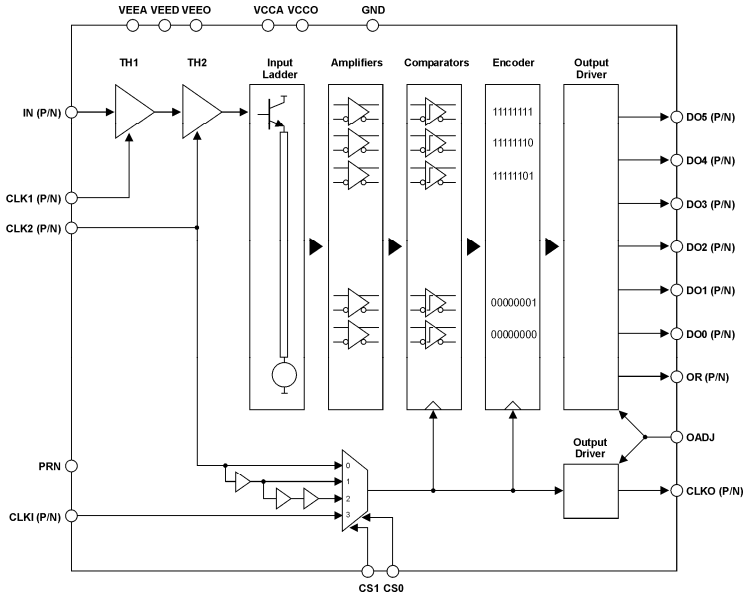

Figure 1 - Functional Block Diagram

Product Description

RAD004 enables 6Bit analog to digital conversion of DC to GHz signals. It has been optimized for ultra-high speed applications with its 4 GS/s operating frequency.
The RAD004's high bandwidth integrated dual track and hold allow the RAD004 to sample signals beyond Nyquist band. Other features include the pseudo random pattern generator, and the ability to select the ADC clock from four settings to optimize performance.

Ordering information

PART NUMBER	DESCRIPTION
RAD004-QP	6 BIT 4GS/s ADC, QFP Package
RAD004-DI	6 BIT 4GS/s ADC, DIE
EVRAD004-QP	RAD004 Evaluation Board

CAUTION
DEVICE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)

Absolute Maximum Ratings

Supply Voltages

Between GNDs ..... -0.3 to +0.3 V
Between VEEs ..... -0.3 to +0.3 V
VCCs to GND ..... -1 V to +6 V
VEEs to GND ..... -6 V to +1 V

RF Input Voltages

INP, INN to GND ..... -1 to +1 V
CLKIP, CLKIN to GND ..... -1 to +1 V
CLK1P, CLK1N to GND ..... -1 to +1 V
CLK2P, CLK2N to GND ..... -1 to +1 V

DC Analog Input Voltages

OADJ to GND ..... -6 to +1 V

DC Digital Input Voltages

CS0, CS1 to GND ..... -6 to +1 V
PRN to GND ..... -6 to +1 V

Output Termination Voltages

DO<0:5>P, DO<0:5>N to GND ..... -6 to +1 V
ORP, ORN to GND ..... -6 to +1 V
CLKOP, CLKON to GND ..... -6 to +1 V

Temperature

Case Temperature (at Heatsink)..... -40 to +85 °C
Junction Temperature..... +125 °C
Lead, Soldering (10 Seconds) ..... +240 °C
Storage..... -60 to 125 °C

DC Electrical Specification

Test Conditions (see notes for specific conditions): Temperature: Room Temperature; VCCA = 5.0V; VCCO = 0V; VEEA = -5.2V; VEED = -5.2V; VEEO = -5.2V; Input Signal: 0.7Vpp Sinewave; Clock: 4GHz, 0.6Vpp Differential; Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
1.0	**DC TRANSFER FUNCTION**						
1.1	Full Scale Range[1]	FSR	Note 1		0.5		V
1.2	Offset Voltage					±15	mV
1.3	Resolution		Grey Code	6		6	bits
1.4	Missing Codes				0		
1.5	Differential Nonlinearity	DNL	Maximum of Absolute Value		0.5	1.2	LSB
1.6	Integral Nonlinearity	INL	Maximum of Absolute Value		1	2	LSB
2.0	**TEMPERATURE DRIFT**						
2.1	Warm-up Time		After Power-up			30	s
2.2	Reference Drift		After Warm-up		TBD		µV/°C
2.3	Gain Drift		After Warm-up		TBD		ppm/°C
2.4	Offset Voltage Drift		After Warm-up		TBD		µV/°C
3.0	**ANALOG SIGNAL INPUTS (INP, INN)**						
3.1	Input Resistance	Z_{IIN}		46	50	54	Ω
3.2	Input Capacitance	C_{IIN}			250		fF
4.0	**CLOCK INPUTS (CLKIP, CLKIN, CLK1P, CLK1N, CLK2P, CLK2N)**						
4.1	Input Resistance	Z_{CIN}		46	50	54	Ω
4.2	Input Capacitance	C_{CIN}			250		fF
5.0	**DIGITAL INPUTS (CS0, CS1)**						
5.1	Input Resistance	R_{DIN}			10K		Ω
6.0	**DIGITAL OUTPUTS (DO<0-5>P, DO<0-5>N, ORP, ORN)**						
6.1	Swing		Into 50 Ω Rterm	0	0.4	0.6	Vpp
7.0	**CLOCK OUTPUTS (CLKOP, CLKON)**						
7.1	Swing		Into 50 Ω Rterm	0	0.4	0.6	Vpp
8.0	**REFERENCE (OADJ)**						
8.1	Input Resistance	R_{OADJ}		150			Ω
9.0	**POWER SUPPLY REQUIREMENTS**						
9.1	Positive Supply Current	ICC			55	70	mA
9.2	Negative Current, Analog	IEEA			260	310	mA
9.3	Negative Current, Digital	IEED			990	1170	mA
9.4	Output Supply Current	IEEO			130	190	mA
9.5	Power Dissipation	P			7.5	8.2	W

[1] Please note that engineering samples have FSR of 1V.

AC Electrical Specification

Test Conditions (see notes for specific conditions): Temperature: Room Temperature; VCCA = 5.0V; VCCO = 0V; VEEA = -5.2V; VEED = -5.2V; VEEO = -5.2V; Input Signal: 0.7Vpp Sinewave; Clock: 4GHz, 0.6Vpp Differential; Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
10.0	**DYNAMIC PERFORMANCE**						
10.1	Input Bandwidth	BW	Large Signal (0.5Vpp) Note 1	6			GHz
10.2	Input Bandwidth	bw	Small Signal (0.1Vpp)	10			GHz
10.3	Aperture Jitter	Δt			100		fs
10.4	SFDR	SFDR 1	60MHz Input		29		dB
10.5	SFDR	SFDR 2	1060MHz Input		30		dB
10.6	SFDR	SFDR 3	2060MHz Input		36		dB
10.7	SFDR	SFDR 4	3060MHz Input		30		dB
10.8	SFDR	SFDR 5	4060MHz Input		30		dB
10.9	SNR	SNR1	60MHz Input		31		dB
10.10	SNR	SNR 2	1060MHz Input		31		dB
10.11	SNR	SNR 3	2060MHz Input		29		dB
10.12	SNR	SNR 4	3060MHz Input		31		dB
10.13	SNR	SNR 5	4060MHz Input		32		dB
10.14	THD	THD 1	60MHz Input		26		dB
10.15	THD	THD 2	1060MHz Input		27		dB
10.16	THD	THD 3	2060MHz Input		32		dB
10.17	THD	THD 4	3060MHz Input		27		dB
10.18	THD	THD 5	4060MHz Input		27		dB
11.0	**DIGITAL OUTPUTS (DO<0-5>P, DO<0-5>N, ORP, ORN)**						
11.1	Delay from CLKI	t_{CIDODL}		90	115	140	ps
11.2	Fall Time	T_{DOF}	20% to 80%		50	80	ps
11.3	Rise Time	T_{DOR}	20% to 80%		50	80	ps
12.0	**CLOCK OUTPUTS (CLKOP, CLKON)**						
12.1	CLKO to Data Out Skew	t_{CODOSK}			-40		ps
12.2	CLKI to CLKO Delay	t_{CICODL}			75		ps

Operating Conditions

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
13.0	**ANALOG SIGNAL INPUTS (INP, INN)**						
13.1	Common Mode Voltage	V_{ICM}		-250	0	250	mV
14.0	**CLOCK INPUTS (CLKIP, CLKIN, CLK1P, CLK1N, CLK2P, CLK2N)**						
14.1	Amplitude	V_{CPP}		200	400	1000	mV
14.2	Common Mode Voltage	V_{CCM}		-250	0	250	mV
14.3	Maximum Frequency	F_{MAX}		4000			MHz
14.4	Minimum Frequency	F_{MIN}				100	MHz
14.5	Fall time	t_{CIF}				5.0	ns
14.6	Rise Time	t_{CIR}				5.0	ns
14.7	CLK2 to CLKI Skew[2]	t_{C2CISK}	Note 2		-60		ps
15.0	**DIGITAL INPUTS (CS0, CS1)**						
15.1	Input High Voltage	V_{IH}		-1.1	0	0	V
15.2	Input Low Voltage	V_{IL}		VEE	VEE	-1.5	V
16.0	**DIGITAL OUTPUTS (DO<0-5>P, DO<0-5>N, ORP, ORN)**						
16.1	Termination Voltage	Vterm		-2.5	0	+3.6	V
16.2	Termination Resistor	Rterm	Required Between Outputs And VCCO		50		Ω
17.0	**CLOCK OUTPUTS (CLKOP, CLKON)**						
17.1	Termination Voltage	Vterm		-2.5	0	+3.6	V
17.2	Termination Resistor	Rterm	Required Between Outputs And VCCO		50		Ω
18.0	**REFERENCE (OADJ)**						
18.1	Reference Voltage	V_{OADJ}		VEE	-1.0	0	V
19.0	**POWER SUPPLY REQUIREMENTS**						
19.1	Positive Supply Voltage	VCCA		4.75	5.0	5.25	V
19.2	Negative Supply Voltage	VEEA, VEED		-5.45	-5.2	-4.95	V
19.3	Output Supply Voltage	VCCO		-1.0	0	2.0	V
19.4	Output Supply Voltage	VEEO		-5.45	VEE	-4.0	V
20.0	**OPERATING TEMPERATURE**						
20.1	Case Temperature	Tc	At Heatsink	-40		85	°C
20.2	Junction Temperature	Tj		0		125	°C

[2] CLKI should be used for maximum performance when operating at high frequencies.

Pin Description

P/I/O	PIN	NUM.	NAME	FUNCTION
P	78, 79	2	VEEA	Analog VEE Power Supply
P	13, 14, 27, 28, 70, 71, 72	7	VEED	Digital VEE Power Supply
P	45, 54, 68	3	VEEO	Output VEE Power Supply
P	80, 81	2	VCCA	VCC Analog Power Supply
P	36, 39, 42, 48, 51, 55, 58, 61, 64, 67	10	VCCO	Output VCC Power Supply
P	1, 3, 6, 9, 12, 15, 20, 23, 69, 73, 75, 77, 87, 88	14	GND	Ground
I	82	1	OADJ	Output Level Adjustment
I	76	1	INP	INP / INN Is Analog Input
I	74	1	INN	
I	21	1	CLKIP	CLKIP / CLKIN Is Clock Input
I	22	1	CLKIN	
I	4	1	CLK1P	CLK1P / CLK1N Is Differential Clock for THA1
I	5	1	CLK1N	
I	7	1	CLK2P	CLK2P / CLK2N Is Differential Clock for THA2
I	8	1	CLK2N	
I	24	1	CS0	Clock Select: CS1 CS0 Clock 0 0 No Delay 0 1 20 ps Delay (typ) 1 0 60 ps Delay (typ) 1 1 CLKI If Floated Default to 11 – Recommended for maximum Performance
I	25	1	CS1	
I	29	1	PRN	Pseudo Random Pattern Generator: Active High
O	40, 43, 46, 52, 56, 59	6	DO<0-5>P	DO<i>P / DO<i>N Is Differential Digital Bit i Output. MSB is bit 5.
O	41, 44, 47, 53, 57, 60	6	DO<0-5>N	
O	37	1	ORP	ORP / ORN Is Differential Digital Out-of-Range Output
O	38	1	ORN	
O	49	1	CLKOP	CLKOP / CLKON Is Differential Output Clock
O	50	1	CLKON	
RES	2, 10,11, 16, 17, 18, 19, 26, 30, 31, 32, 33, 34, 35, 62, 63, 65, 66, 83, 84, 85, 86	18	RES	Reserved

Pin Layout (TOP view)

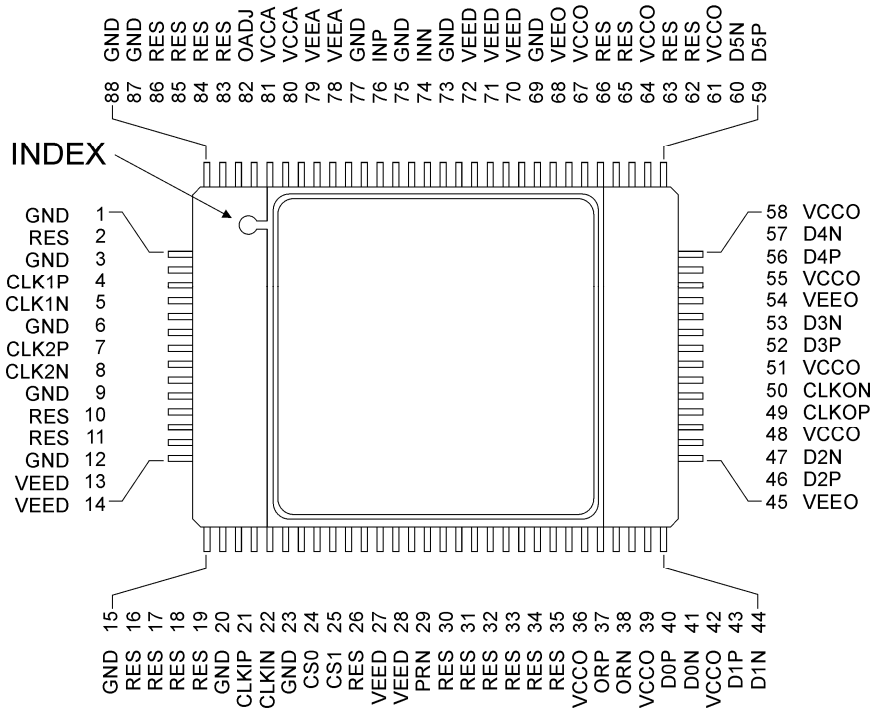

Figure 2 - RAD004-QP pinout (top view).

Theory of Operation

The RAD004 consists of a track and hold (T/H), interpolating amplifiers, a flash digitizer and supporting circuitry, including clock timing and Pseudo Random Number (PRN) generation. Operation with optimized clocks will result in an unprecedented 4GS/sec with input signals up to 4GHz.

T/H clocks

The T/H samples the analog input signal and holds the input for the digitizer circuitry. Two clocks are used, one for the master T/H and one for the slave T/H. The jitter on the master T/H is critical, since jitter on this clock will translate into noise on the sampled signal according to:

$$V_{rms} = \frac{2\ p\ F\ A\ T_{jrms}}{Sqrt(2)}$$

A = input amplitude
F = input frequency
T_{jrms} = RMS jitter at the bridge

To achieve a 6 bit noise level at 4 GHz, we see we require 879fsrms jitter. The input buffers on the RAD004 have been seen to have less than 130fs additive jitter. A differential square wave with very high edge rates is best for low noise, but sine waves may be used. The low edge rate of low frequency sinewaves is detrimental to jitter generation. Furthermore, the small hold capacitors in the master T/H limit the clock rate to a minimum of 100MHz.

The slave T/H (CLK2) is far less critical, since it only affects timing margins and does not add noise to the input signal. All clocks have precision 50 ohm terminations to GND.

Digitizer Clock

CLKI is the clock to the digitizer (and the PRN). For optimal performance, the phase of CLKI must be optimized with respect to CLK2, with 60ps lead time being about optimal. This delay is easily built into the traces on the PCB. The clock select inputs (CS0, CS1) are both high (GND) for this mode of operation. For relaxed sample frequency, say 3Ghz, the margins are wider and the criticality of this phase is reduced. One may drive the RAD004 with a single pair of differential clocks, in this case, by driving CLK1 with clock, CLK2 with clock bar, and setting CS0 = CS1 = VEE.

Interpolating amplifiers and digitizer

The held signal from the T/H is applied to a resistive ladder which drives interpolating amplifiers. The amplifiers are employed both to limit the capacitive load on the resistive ladder, and to provide the high gains needed by the digitizer. A conventional flash digitizer and grey code encoder is employed. Grey code offers a single bit transition for adjacent codes, and minimizes digitally generated noise for low bandwidth inputs. At high output rates, the advantage of grey code is minimal. The RDX004M4 is a glueless companion part that also translates grey code to binary, if desired. When utilizing the RDX004M4 with the RDA004, the output data rate is reduced to 1GBPS.

PRN

The PRN feature is provided to allow the designer to insure the data paths are error free. A 2^{10}-1 pattern is applied to the data outputs when PRN = GND. All outputs transition simultaneously, with a fairly broadband pattern, which will simulate a worst case PCB environment. The pattern is easily checked for accuracy by checking it with a Q0 = XOR(Q2, Q9) polynomial. The PRN section draws no power when disabled.

Equivalent Circuit

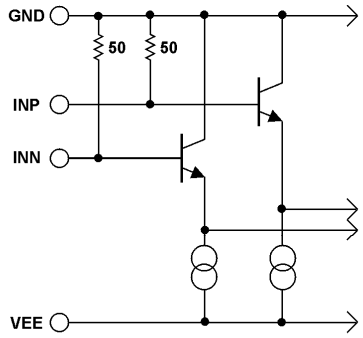

Figure 3 - Analog Input

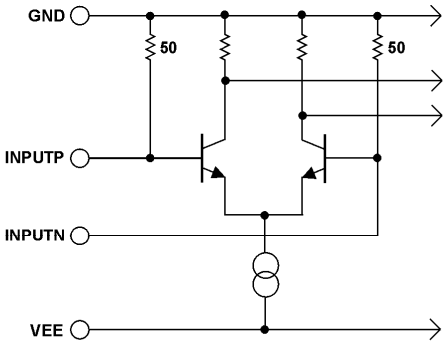

Figure 4 – CLK1, CLK2 Inputs

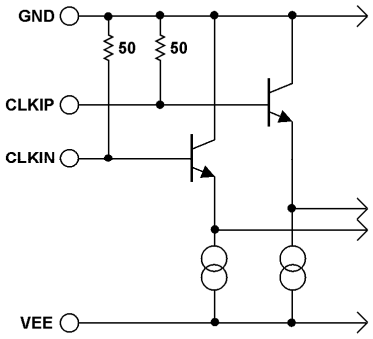

Figure 5 – CLKI Input

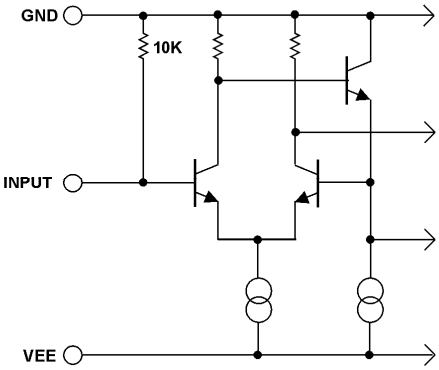

Figure 6 – CS0, CS1, PRN Inputs

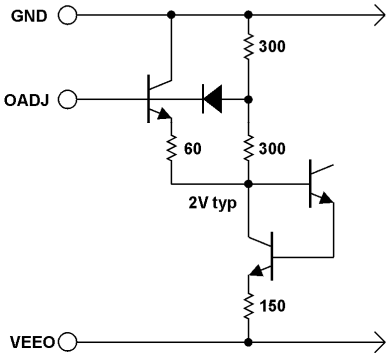

Figure 7 – OADJ Input

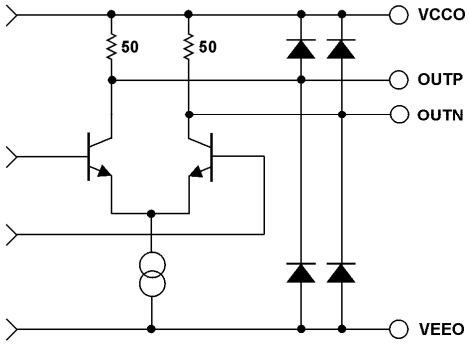

Figure 8 – CLKO, DATA, OR Outputs

Typical Circuit

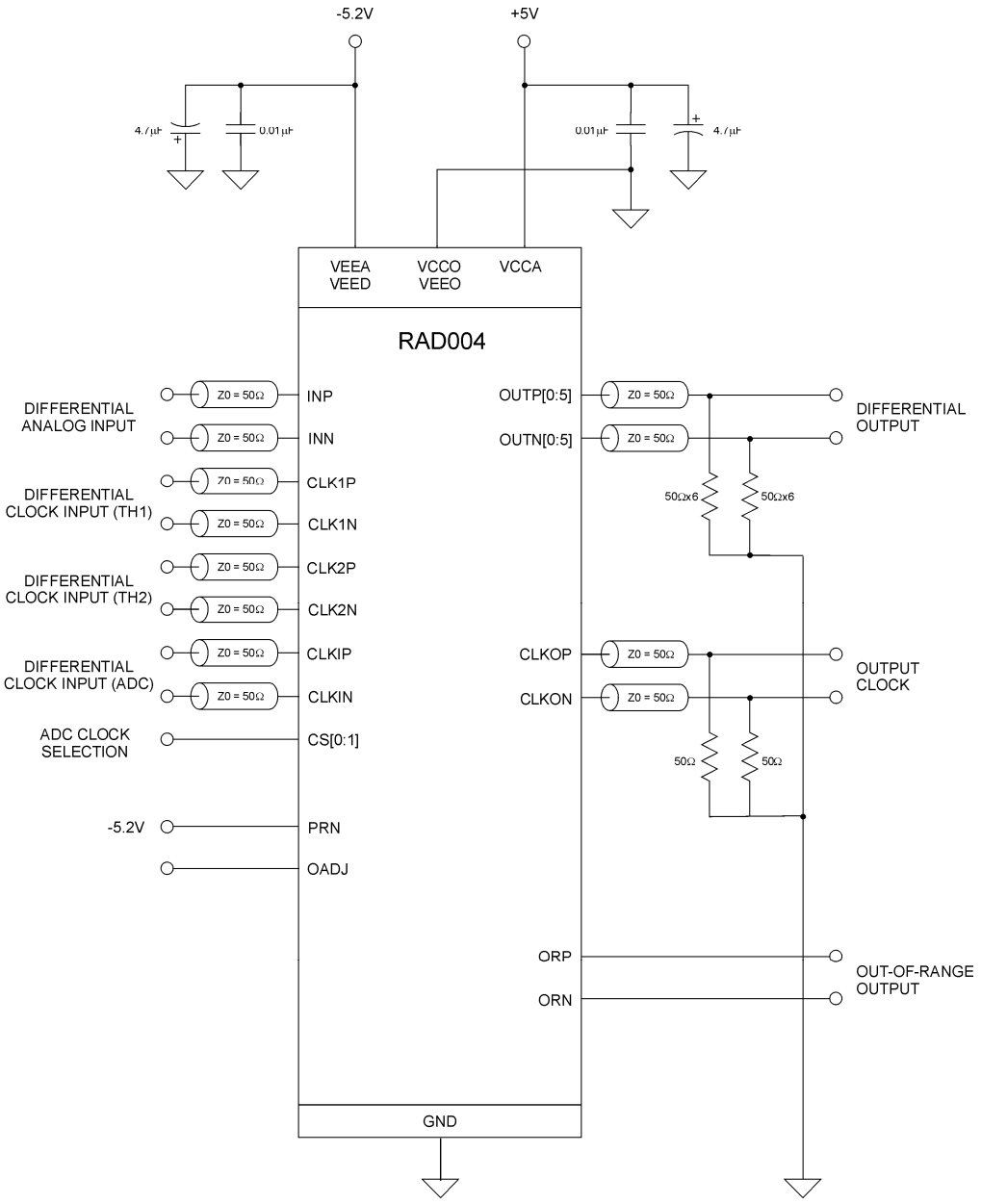

Figure 9 – Typical Operating Circuit

Timing

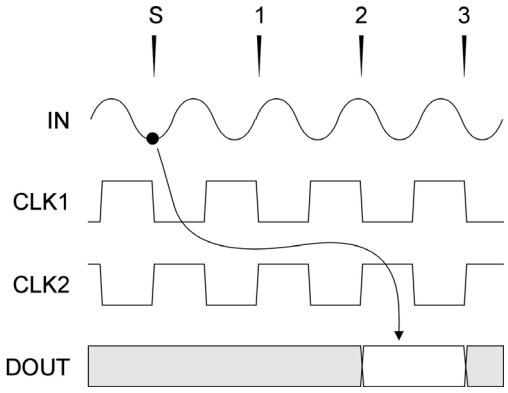

Figure 10 – Latency (CS0=0, CS1=0)

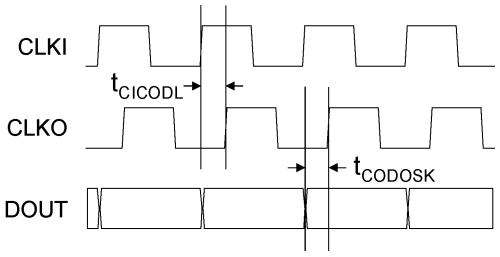

Figure 11 – Data Out timing (CS0=1, CS1=1)

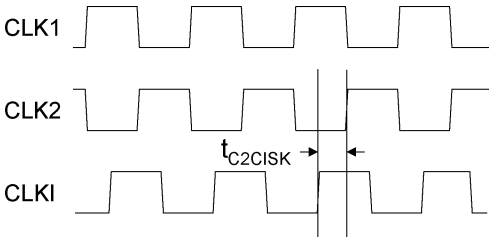

Figure 12 – Input Clock timing (CS0=1, CS1=1)

Package Information

The package is a 88 lead ceramic Quad Flat Pack (QFP) with a heat sink slug on the package's bottom. The leads are trimmed to 0.045 inch (1.15mm) length (from the package edge). The thermal impedance (junction to base) is approximately 3.5 °C/W.

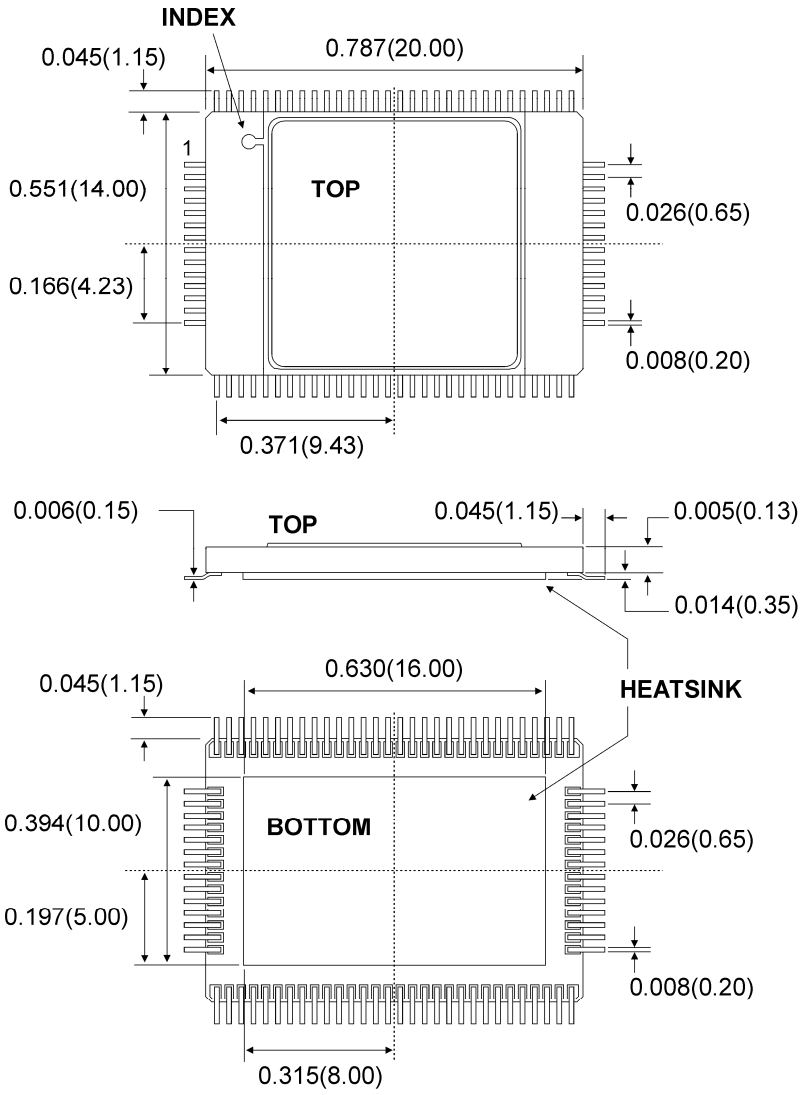

Figure 13 - RAD004-QP package, dimensions shown in inches (mm).