TELEDYNE
SCIENTIFIC COMPANY

RDA012

12 Bit 1.1 GS/s DAC

REV-DATE PD1-2412
FILE DS_0008PD1-2412

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RDA012

12 Bit 1.1 GS/s DAC

Features

- 12 Bit Resolution
- 1.1 GS/s Sampling Rate
- 10 Bit Static Linearity
- 66dB SFDR with Fclk = 1.1GHz, Fout = 370MHz and 100MHz Bandwidth
- ECL Compatible Data Inputs
- Differential Analog Output
- Input code format: Offset Binary
- Output Swing: 600 mV with 50 Ω Termination to GND
- Differential ECL or Sinusoidal Clock Input
- Reference Output/Input Pin for Accurate Full-Scale Adjustment.
- -5.2V Power Supply
- 32 Lead QFP package

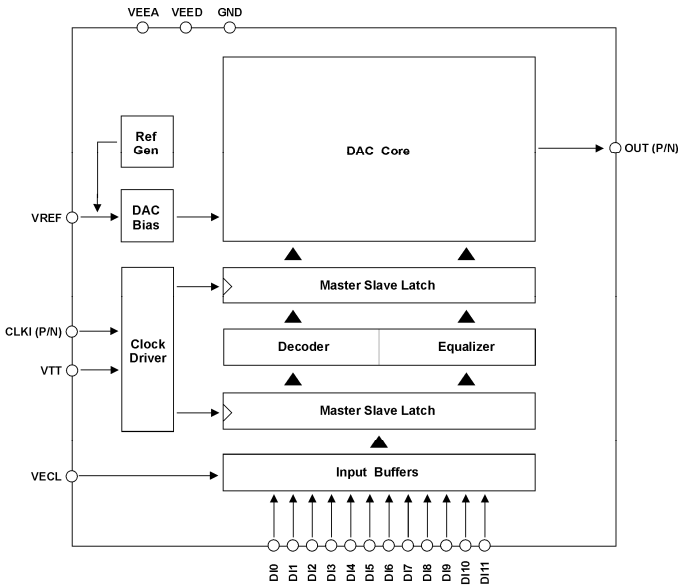

Figure 1- Functional Block Diagram

Product Description

The RDA012 is a high performance 12 Bit digital to analog converter (DAC) with a data update rate over 1.1 GS/s. Fabricated in an 80 GHz f_T GaAs HBT process, the RDA012 has been optimized for ultra-high speed applications, achieving 66dB of spurious-free dynamic range (SFDR) at 1.1 GS/s, with Fout of 370MHz and 100MHz of bandwidth. The DAC utilizes a segmented current source to reduce glitch energy and to achieve high linearity performance. For better dynamic performance, the DAC outputs are internally terminated with 50Ω resistance. It outputs a nominally full-scale current of 12mA when terminated with external 50Ω resistors.

Ordering information

PART NUMBER	DESCRIPTION
RDA012-QP	12 BIT 1.1GS/s DAC, QFP Package
RDA012-DI	12 BIT 1.1GS/s DAC, DIE
EVRDA012-QP	RDA012 Evaluation Board

CAUTION
DEVICE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)

Absolute Maximum Ratings

Supply Voltages
VEEs to GND..... -6 V to 1 V

RF Input Voltages
CLKIP, CLKIN ……..……. -3 V to 1 V

Digital Input Voltages
DI<0:11>……..... -6 V to 1 V

Output Termination Voltages
OUTP, OUTN…….....-1 V to 1 V

Temperature
Case Temperature……-40 to 85 °C
Junction Temperature……..125 °C
Lead, Soldering (10 Seconds).....……..220 °C
Storage……...…-40 to 125 °C

DC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VEEA = -5.2V; VEED = -5.2V; VREF = -2V; VECL = -1.3V; Clock: 1.1GHz, 0.6Vpp Differential; Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
1.0	**DC TRANSFER FUNCTION**						
1.1	Differential Nonlinearity	DNL	Maximum of Absolute Value		4		LSB
1.2	Integral Nonlinearity	INL	Maximum of Absolute Value		4		LSB
2.0	**TEMPERATURE DRIFT**						
2.1	Warm-up Time		After Power-up			30	s
3.0	**CLOCK INPUT (CLKIP, CLKIN)**						
3.1	Input Resistance	Z_{CIN}	Resistance to VTT	45	50	55	Ω
3.2	Input Capacitance	C_{CIN}			250		fF
4.0	**DIGITAL INPUTS (DI<0:11>)**						
4.1	Input Resistance	R_{DIN}			10K		Ω
5.0	**ANALOG OUTPUTS (OUTP, OUTN)**						
5.1	Swing		Single Ended Into 50Ω to GND		600		mVpp
6.0	**REFERENCE (VREF)**						
6.1	Input Resistance	R_{VREF}			560		Ω
6.2	Reference Voltage	V_{VREF}	Output from Internal Reference		-2		V
7.0	**POWER SUPPLY REQUIREMENTS**						
7.1	Power Dissipation	P			1.8		W

AC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VEEA = -5.2V; VEED = -5.2V; VREF = -2V; VECL = -1.3V; Clock: 1.1GHz, 0.6Vpp Differential; Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
8.0	**DYNAMIC PERFORMANCE[1] (note 1)**						
8.1	SFDR	SFDR 1	52MHz Input[1]		66		dB
8.2	SFDR	SFDR 2	252MHz Input[1]		54		dB
8.3	SFDR	SFDR 3	340MHz Input[1]		54		dB
8.4	SFDR	SFDR 4	52MHz Input, 100MHz BW[1]		76		dB
8.5	SFDR	SFDR 5	340MHz Input, 100MHz BW[1]		66		dB

[1] Items 8.1, 8.2, 8.3 were measured using full Nyquist. Items 8.4 and 8.5 were measured using a 100MHz band centered at Fout.

Operating Conditions

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
9.0	**CLOCK INPUTS (CLKIP, CLKIN)**						
9.1	Amplitude	V_{CPP}		400	600	800	mV
9.2	Common Mode Voltage	V_{CCM}		-0.8	-1.5	-2	V
9.3	Maximum Frequency	F_{MAX}		1100			MHz
10.0	**DIGITAL INPUTS (DI<0:11>)**						
10.1	Input High Voltage	V_{IH}	V_{ECL} = -1.3V	-1.15	-0.95	-0.3	V
10.2	Input Low Voltage	V_{IL}	V_{ECL} = -1.3V	-2.2	-1.75	-1.45	V
11.0	**TERMINATION VOLTAGE (VTT)**						
11.1	Reference Voltage	V_{TT}	Termination Voltage for CLKI		-2		V
12.0	**REFERENCE (VECL)**						
12.1	Reference Voltage	V_{ECL}	Reference Voltage for DI<0:11>	-2	-1.3	-0.5	V
13.0	**REFERENCE (VREF)[2] (note 2)**						
13.1	Reference Voltage	V_{REF}		-2.5	-2	-1.2	V
14.0	**POWER SUPPLY REQUIREMENTS**						
14.1	Analog Supply Voltage	VEEA		-5.45	-5.2	-4.95	V
14.2	Digital Supply Voltage	VEED		-5.45	-5.2	-4.95	V
15.0	**OPERATING TEMPERATURE[3] (note 3)**						
15.1	Case Temperature	Tc	Measured at Bottom Plate	-15		85	°C
15.2	Junction Temperature	Tj				125	°C

[2] The DAC core current is generated from an internal reference that is both temperature and supply dependent. The Internal reference can change up to ±2% by changing the supply voltage within the specified range. It can also change up to ±5% according to operating temperature changes. The change in temperature and supply can be minimized by using a precision external voltage reference source connected to VREF.

[3] The part is designed to function with a junction temperature up to 125°C. For the best performance, operation within the specified temperature range with a proper heatsink attached to the device is recommended. The heatsink should be attached to the bottom of the PCB, on a metal pad connect by thermal vias to the metal pad where the part is soldered.

Pin Description and Layout

P/I/O	PIN	NUM.	NAME	FUNCTION
P	19, 20, 21, 22	4	VEEA	-5.2V Analog Power Supply
P	13, 27	2	VEED	-5.2V Digital Power Supply
P	10, 16, 17, 18, 23, 24, 25	7	GND	Ground
P	Bottom Plate	-	GND	Ground
I/O	26	1	VREF	-2V Reference Voltage
I	31	1	VECL	Digital Input Reference
I	29	1	VTT	CLKI Clock Termination Voltage
I	28	1	CLKIP	Clock Input
I	30	1	CLKIN	
I	32, 1, 2, 3, 4, 5, 6, 7, 8, 9, 11, 12	12	DI<0:11>	DI<i> Is Digital Bit i Input. MSB is bit 11
O	15	1	OUTP	Analog Output
O	14	1	OUTN	

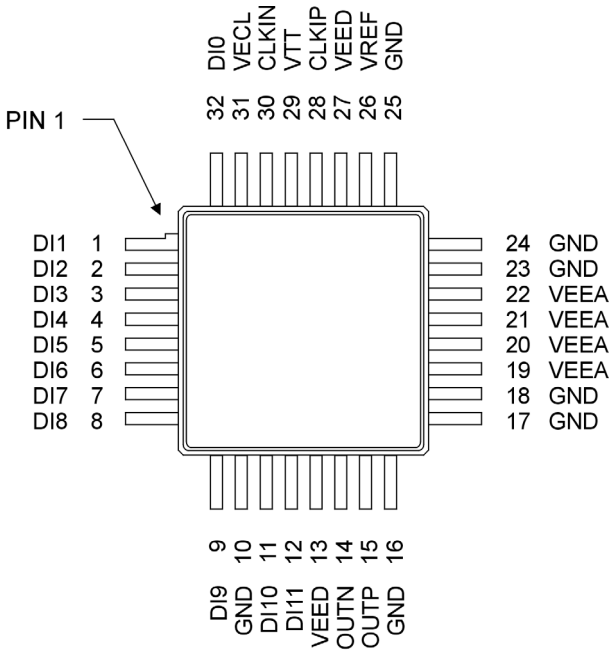

Figure 2 - RDA012-QP pinout (top view).

Pad Layout

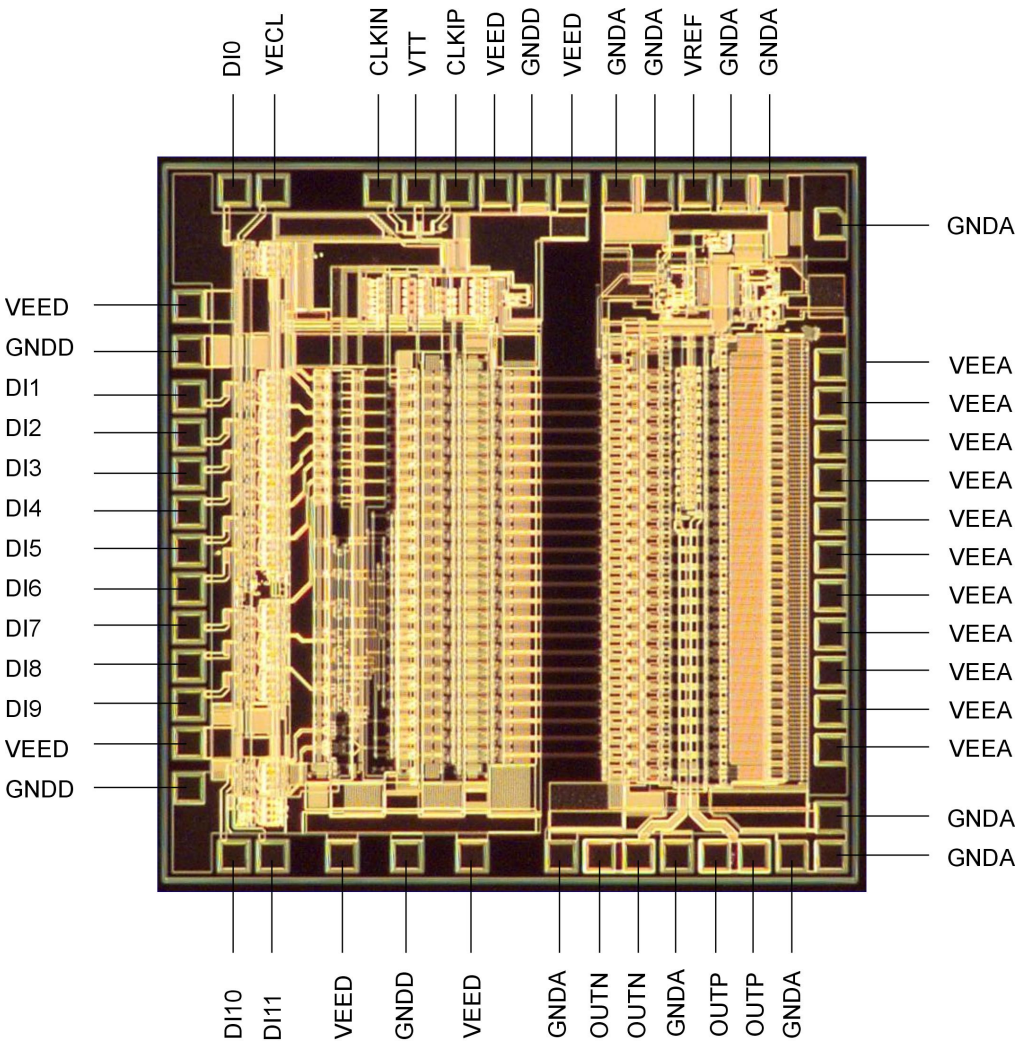

Figure 3 - RDA012 pad layout. Die size is 2650 x 2740 µm.

Theory of Operation

For best dynamic and static performance, the RDA012 DAC employs 4 Bit segmentation. The ECL compatible 12 Bit digital data inputs are latched by master-slave flip-flops immediately after the input buffer to reduce the data skew. The 4 MSB data bits are decoded into thermometer code by a two-stage decoding block, and the 8 LSB data bits are transported through the delay equalizer block. The digital data are then synchronized again by a second master-slave flip-flop to reduce the switching glitch. The decoded 4 MSB data drive 15 identical current switches, and the 8 LSB data drive 8 current switches. The output nodes from the LSB current switches are connected to the analog output through an R-2R ladder to generate the binary output. The RDA012 DAC provides output terminated at 50Ω, illustrated in an equivalent circuit in Figure 5. The output full-scale voltage follows the relationship V_{FS} = 0.3x$V_{REF.}$ An internal reference circuit with approximately -10dB supply rejection is integrated on chip for application convenience, and the reference pin is provided for monitoring and for bypass purposes. To band-limit the noise on the reference voltage, the reference pin should be bypassed to the GND with capacitance > 100pF. The VREF pin can also be used to override the internal reference with an accurate, temperature-compensated external voltage reference.

Equivalent Circuit

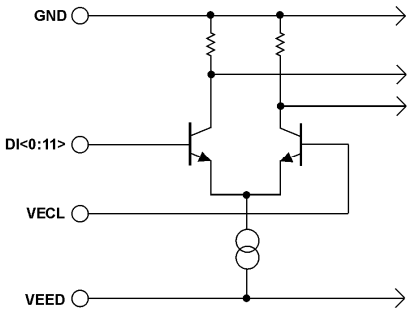

Figure 4 – Data input circuit

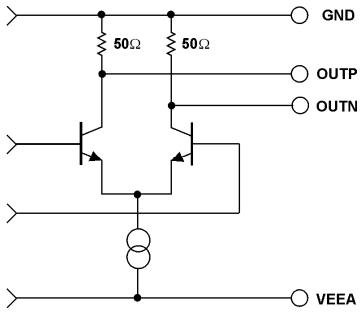

Figure 5 – Output circuit

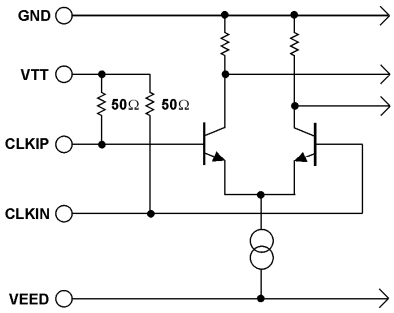

Figure 6 – Clock input circuit

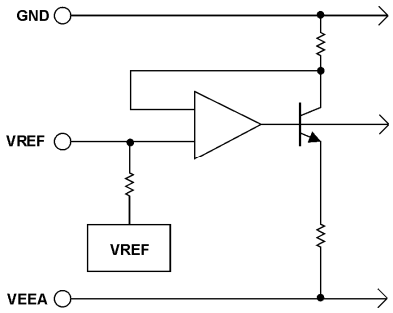

Figure 7 – VREF circuit

Signal Description

HIGH SPEED INPUT CLOCK.

The RDA012 DAC high-speed clock input is differential and can be driven from typical ECL circuits. Also a differential sinusoidal clock can be used. The CLKIP and CLKIN inputs, are internally terminated with 50Ω to VTT which should be connected to a well decoupled –2.0V supply. Since the DAC's output phase noise is directly related to the input clock noise and jitter, a low-jitter clock source is ideal. The internal clock driver generates very little added jitter (~100fs).

DATA INPUT.

The data inputs are single ended ECL compatible. VECL is used as a voltage reference for the data input buffers (Figure 4).

ANALOG OUTPUT.

The outputs OUTP and OUTN should both be connected though a 50Ω resistor to ground. This will give a full-scale amplitude of 0.6 volt (both outputs must be terminated), 1.2 volt differentially. The output common mode can be changed by terminating the load resistors to a different voltage. However, the device is optimized to perform best when connected to a voltage between 0 and 1 volt. For reliable operation, the output termination voltage should not exceed 3 volts.

REFERENCE.

VREF is provided for added control of the full-scale amplitude output. The internal reference circuit is designed to provide -2.0V, which can change up to ±5% as the supply voltage and/or operating temperature changes. If the user prefers accurately control the output full-scale signal, an external voltage reference with low output impedance to override the internal reference should be used. The output full-scale voltage follows the relationship $V_{FS} = 0.3xV_{REF}$. Note that the RDA012 DAC is optimized to have the best performance with a reference voltage of -2.0V. The output resistance of the reference node is 560 Ω ±10%.

Typical Operating Circuit

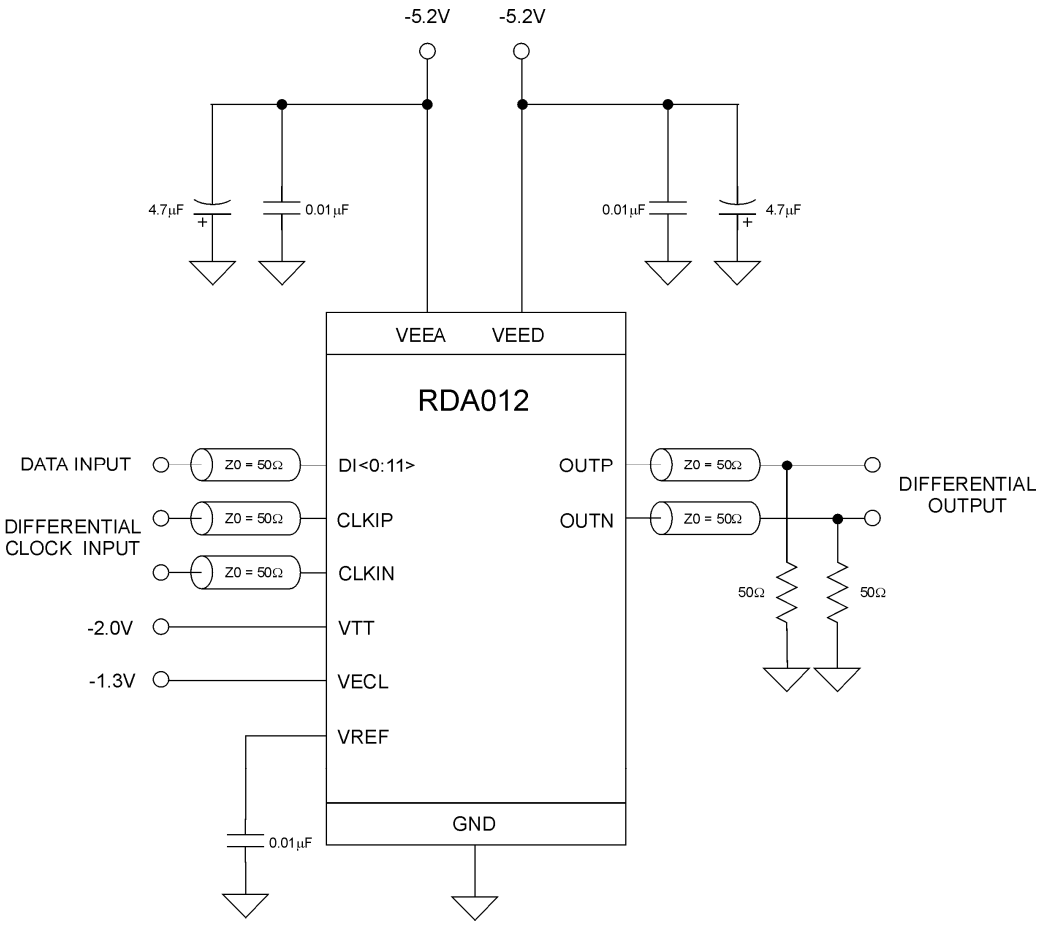

Figure 8 - RDA012 typical operating circuit using the internal voltage reference.

Typical Performance

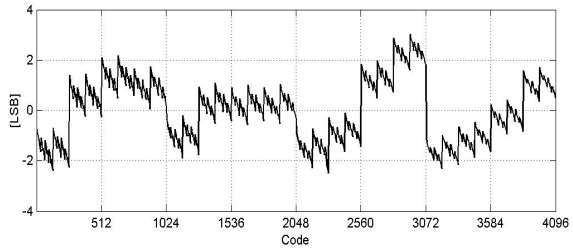

Figure 9– RDA012 INL

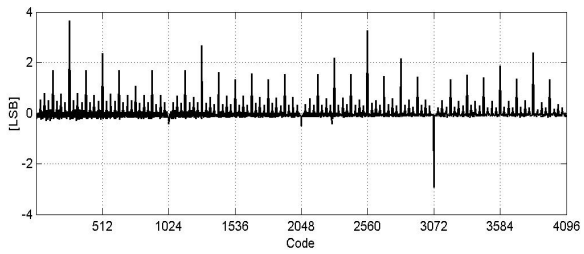

Figure 10 – RDA012 DNL

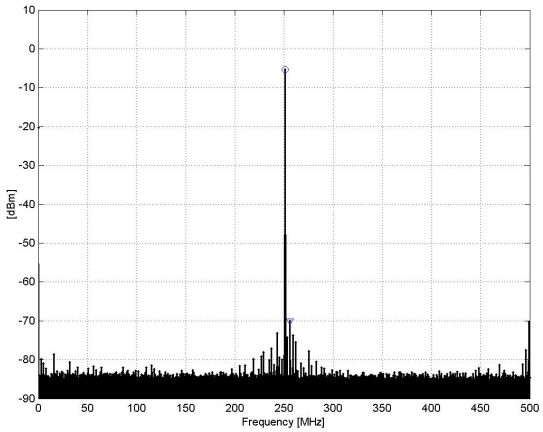

Figure 11 – Spectrum at Fclk=1GHz, Fout=250MHz

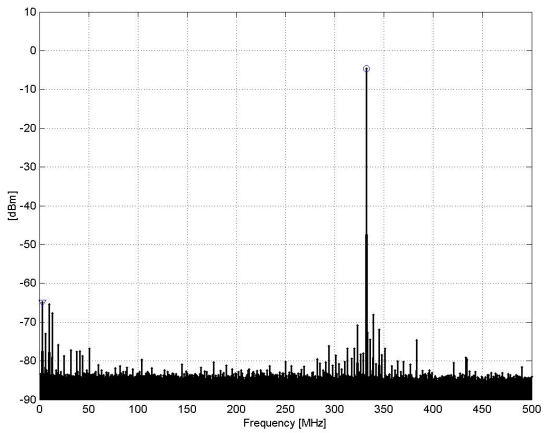

Figure 12 – Spectrum at Fclk=1GHz, Fout=333MHz

Package Information

The package is a 32 lead metal ceramic base, glass sidewall Quad Flat Pack (QFP) with a heatsink slug on the package's bottom. The leads are gull-winged formed.

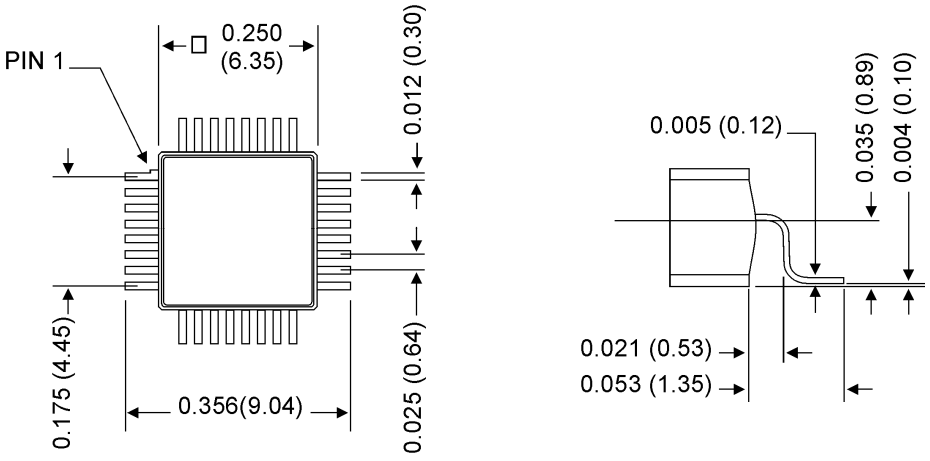

Figure 13 - RDA012-QP package, dimensions shown in inches (mm).

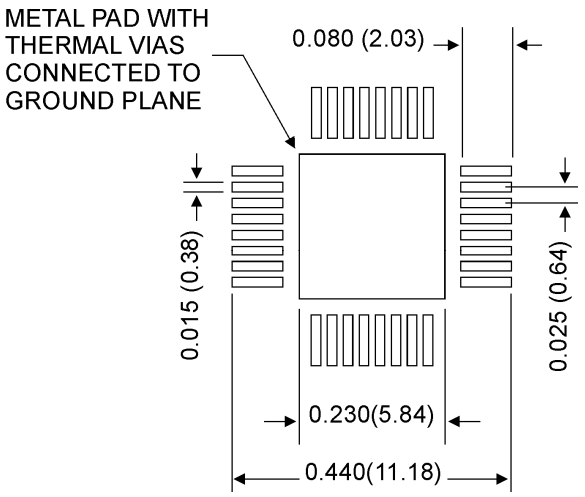

Figure 14 - RDA012-QP footprint, dimensions shown in inches (mm).