TELEDYNE
SCIENTIFIC COMPANY

RDA012M4MS

12 Bit 1.3 GS/s Master-Slave 4:1 MUXDAC

REV-DATE PB3-2412
FILE DS_0017PB3-2412

DS

RDA012M4MS

12 Bit 1.3 GS/s Master-Slave 4:1 MUXDAC

Features

- 12 Bit Resolution
- 1.3 GS/s Sampling Rate
- 4:1 Input Multiplexer
- Master-Slave Operation for Synchronous Operation of Multiple Devices
- Differential Analog Output
- Input Code Format: Offset Binary
- Output Swing: 600 mV with 50 Ω Termination
- 3.3V NMOS-Compatible Data Inputs
- Differential ECL or Sinusoidal Clock Input
- LVDS Compatible Clock Output
- 10 Bit Static Linearity
- Reference Output/Input Pin for Accurate Full-Scale Adjustment.
- 3.3V and -5.2V Power Supply
- 77 Lead HSD or 88 Lead QFP Package

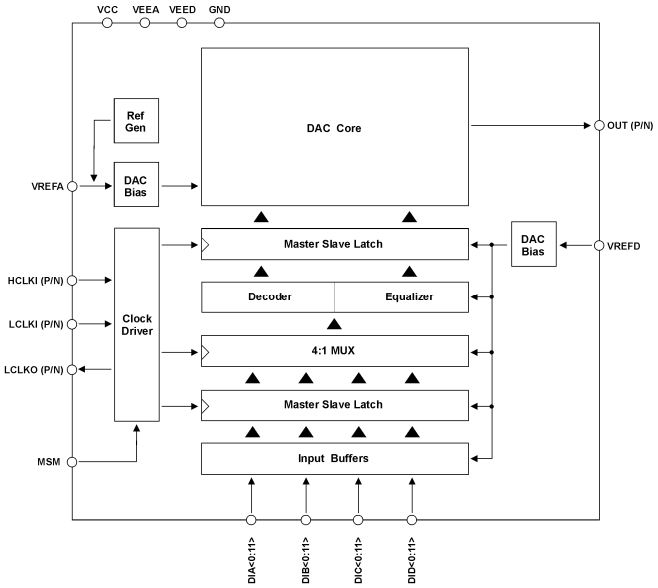

Figure 1 - Functional Block Diagram

Product Description

The RDA012M4MS is a digital-to-analog converter (DAC) with a 4:1 input multiplexer and a maximum update rate of 1.3GS/s. The RDA012M4MS features master-slave operation that simplifies synchronization when multiple devices are required, such as in an I-Q modulation scheme. The integrated DAC utilizes a segmented current source to reduce the glitch energy and achieve high linearity performance. For best dynamic performance, the DAC outputs are internally terminated with 50Ω resistance, and outputs a nominal full-scale current of 12mA when terminated with external 50Ω resistors. For a convenient interface with most CMOS ICs, the digital data inputs are low voltage NMOS compatible.

Ordering information

PART NUMBER	DESCRIPTION
RDA012M4MS-DI	12 BIT 4:1 MUX 1.3GS/s DAC, DIE
RDA012M4MS-HD	12 BIT 4:1 MUX 1.3GS/s DAC, 77 Lead HSD Package
RDA012M4MS-QP	12 BIT 4:1 MUX 1.3GS/s DAC, 88 Lead QFP Package
EVRDA012M4MS-HD	RDA012M4MS-HD Evaluation Board
EVRDA012M4MS-QP	RDA012M4MS-QP Evaluation Board

CAUTION
DEVICE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)

The "-QP" products represented in this datasheet are regulated under the International Traffic in Arms Regulations (ITAR)
Public Domain Information – Previously Approved for Public Release (DOD Office of Security Review, Case 08-S-0596)

Absolute Maximum Ratings

Supply Voltages

Between GNDs ..... -0.3V to +0.3V
Between VCCs ..... -0.3V to +0.3V
VCCs to GND ..... 0V to +3.8V

RF Input Voltages

CLKIP, CLKIN to GND ..... -3 V to 1 V

HS Digital Input Voltages

DI<0:11> ..... 0V to VCC

Output Termination Voltages

OUTP, OUTN to GND ..... -1 V to 1 V

Temperature

Case Temperature..... -40 to +85 °C
Junction Temperature..... +125 °C
Lead, Soldering (10 Seconds) ..... +220 °C
Storage..... -60 to 125 °C

DC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VCC = 3.3V; VEEA = -5.2V; VEED = -5.2V; VREFA = -2V; VREFD = -2V; Clock: 1.3GHz, 0.6Vpp Differential; Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
1.0	**DC TRANSFER FUNCTION**						
1.1	Differential Nonlinearity	DNL	Maximum of Absolute Value		4		LSB
1.2	Integral Nonlinearity	INL	Maximum of Absolute Value		4		LSB
2.0	**TEMPERATURE DRIFT**						
2.1	Warm-up Time		After Power-up			30	s
3.0	**HIGH CLOCK INPUT (HCLKIP, HCLKIN)**						
3.1	Input Resistance	R_{CIN}	Resistance to VTT	45	50	55	Ω
4.0	**DIGITAL INPUTS (DIA<0:11>, DIB<0:11>, DIC<0:11>, DID<0:11>)**						
4.1	Input Resistance	R_{DIN}			2K		Ω
5.0	**LOW CLOCK INPUT (LCLKIP, LCLKIN)**						
5.1	Input Resistance	R_{LCIN}	Differential LVDS		100		Ω
6.0	**LOW CLOCK OUTPUT (LCLKOP, LCLKON)**						
6.1	Common Mode	$V_{CM,LCKO}$		0.9	1.2	1.5	V
6.2	Amplitude Voltage	$V_{CPP,LCKO}$	Differential LVDS	250	350	450	mV
7.0	**ANALOG OUTPUTS (OUTP, OUTN)**						
7.1	Full-scale Output Swing	V_{FSD}	Differential, Terminated Into 50Ω to GND on Each Output	1140	1200	1260	mVpp
7.2	Full-scale Output Swing	V_{FSS}	Single Ended, Terminated Into 50Ω to GND	570	600	630	mVpp
7.3	Full-scale Output Range	V_{FSRS}	Single Ended, Terminated Into 50Ω to GND (MIN=000h, MAX=FFFh)	-650		0	V
7.4	Output Current	I_{OUT}	Terminated Into 50Ω to GND		12		mA
8.0	**ANALOG REFERENCE (VREFA)**						
8.1	Reference Voltage	V_{VREFA}	Output from Internal Reference	-1.9	-2	-2.1	V
9.0	**DIGITAL REFERENCE (VREFD)**						
9.1	Reference Voltage	V_{VREFD}	Output from Internal Reference	-1.9	-2	-2.1	V
10.0	**POWER SUPPLY REQUIREMENTS**						
10.1	Positive Current	ICC			150		mA
10.2	Negative Current, Analog	IEEA			95		mA
10.3	Negative Current, Digital	IEED			420		mA
10.4	Power Dissipation	P	Total Dissipation		3.3		W
10.5	Power Dissipation	P_{VCC}	Positive Supply		0.5		W
10.6	Power Dissipation	P_{VEEA}	Negative Supply, Analog		0.5		W
10.7	Power Dissipation	P_{VEED}	Negative Supply, Digital		2.3		W

AC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VCC = 3.3V; VEEA = -5.2V; VEED = -5.2V; VREFA = -2V; VREFD = -2V; Clock: 1.3GHz, 0.6Vpp Differential; Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
11.0	**DYNAMIC PERFORMANCE**						
11.1	SFDR	SFDR 1	F_{CLK} = 800MHz, F_{OUT} = 267MHz		56		dBc
11.2	SFDR	SFDR 2	F_{CLK} = 1GHz, F_{OUT} = 333MHz		53		dBc
11.3	SFDR	SFDR 3	F_{CLK} = 1.3GHz, F_{OUT} = 400MHz		50		dBc
12.0	**DATA TIMING (DIA<0:11>, DIB<0:11>, DIC<0:11>, DID<0:11>)**						
12.1	Data In to LCLKO Setup	$t_{DTLCKST}$		300			ps
12.2	Data In to LCLKO Hold	$t_{DTLCKHD}$		-50			ps

Operating Conditions

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
13.0	**HIGH CLOCK INPUT (HCLKIP, HCLKIN)**						
13.1	Amplitude	V_{CPP}	Differential ECL	400	600	800	mV
13.2	Common Mode Voltage	V_{CCM}		-0.8	-1.5	-2	V
13.3	Maximum Frequency	F_{MAX}		1300			MHz
13.4	Minimum Frequency	F_{MIN}				1	MHz
14.0	**LOW CLOCK INPUT (LCLKIP, LCLKIN)**						
14.1	Amplitude	V_{LCPP}	Differential LVDS	250	350	450	mV
14.2	Common Mode Voltage	V_{LCCM}		0.9	1.2	1.5	V
15.0	**DIGITAL INPUTS (DIA<0:11>, DIB<0:11>, DIC<0:11>, DID<0:11>)**						
15.1	Input High Voltage	V_{IH}		0.9		VCC	V
15.2	Input Low Voltage	V_{IL}		-0.4		0.4	V
16.0	**TERMINATION VOLTAGE (VTT)**						
16.1	Termination Voltage	V_{TT}	Termination Voltage for HCLKI		-2		V
17.0	**ANALOG REFERENCE (VREFA)[1] (note 1)**						
17.1	Reference Voltage	V_{REF}		-2.5	-2	-1.2	V
18.0	**DIGITAL REFERENCE (VREFD)**						
18.1	Reference Voltage	V_{REF}		-2.5	-2	-1.2	V
19.0	**POWER SUPPLY REQUIREMENTS**						
19.1	Positive Supply Voltage	VCC		3.1	3.3	3.5	V
19.2	Analog Supply Voltage	VEEA		-5.4	-5.2	-5.0	V
19.3	Digital Supply Voltage	VEED		-5.4	-5.2	-5.0	V
20.0	**OPERATING TEMPERATURE[2] (note 2)**						
20.1	Case Temperature	Tc	Measured at Bottom Plate	-40		85	°C
20.2	Junction Temperature	Tj				125	°C

[1] The DAC core current is generated from an internal reference that is both temperature and supply dependent. The Internal reference can change up to ±2% by changing the supply voltage within the specified range. It can also change up to ±5% according to operating temperature changes. The change in temperature and supply can be minimized by using a precision external voltage reference source connected to VREFA.

[2] The part is designed to function with a junction temperature up to 125°C. For the best performance, operation within the specified temperature range with a proper heatsink attached to the device is recommended. The heatsink should be attached to the bottom of the PCB, on a metal pad connect by thermal vias to the metal pad where the part is soldered.

Pin Description and Pin Layout (HSD Package)

P/I/O	PIN	NUM.	NAME	FUNCTION
P	7, 14, 39, 62	4	VCC	+3.3V Digital Power Supply
P	68, 71, 72, 73, 74, 75, 76	7	VEEA	-5.2V Analog Power Supply
P	8, 12, 26, 52, 64, 67	6	VEED	-5.2V Digital Power Supply
P	Bottom Plate	-	GND	Ground
I	77	1	VREFA	-2V Reference Voltage
I	10	1	VREFD	Digital Circuitry Bias Reference. Bypass to Ground
I	4	1	VTT	HCLKI Clock Termination Voltage
I	6	1	MSM	Master-Slave Mode Selection: Float - Master GND - Slave
I	5	1	HCLKIP	Clock Input
I	3	1	HCLKIN	
I	24	1	LCLKIP	Low Clock Input
I	25	1	LCLKIN	
I	2	1	LCLKOP	Low Clock Output
I	1	1	LCLKON	
I	9, 16, 20, 27, 31, 35, 40, 44, 48, 53, 57, 61	12	DIA<0:11>	DIA<i> Is Channel A Digital Bit i Input. MSB is bit 11
I	11, 17, 21, 28, 32, 36, 41, 45, 49, 54, 58, 63	12	DIB<0:11>	DIB<i> Is Channel B Digital Bit i Input. MSB is bit 11
I	13, 18, 22, 29, 33, 37, 42, 46, 50, 55, 59, 65	12	DIC<0:11>	DIC<i> Is Channel C Digital Bit i Input. MSB is bit 11
I	15, 19, 23, 30, 34, 38, 43, 47, 51, 56, 60, 66	12	DID<0:11>	DID<i> Is Channel D Digital Bit i Input. MSB is bit 11
O	70	1	OUTP	Differential Output
O	69	1	OUTN	

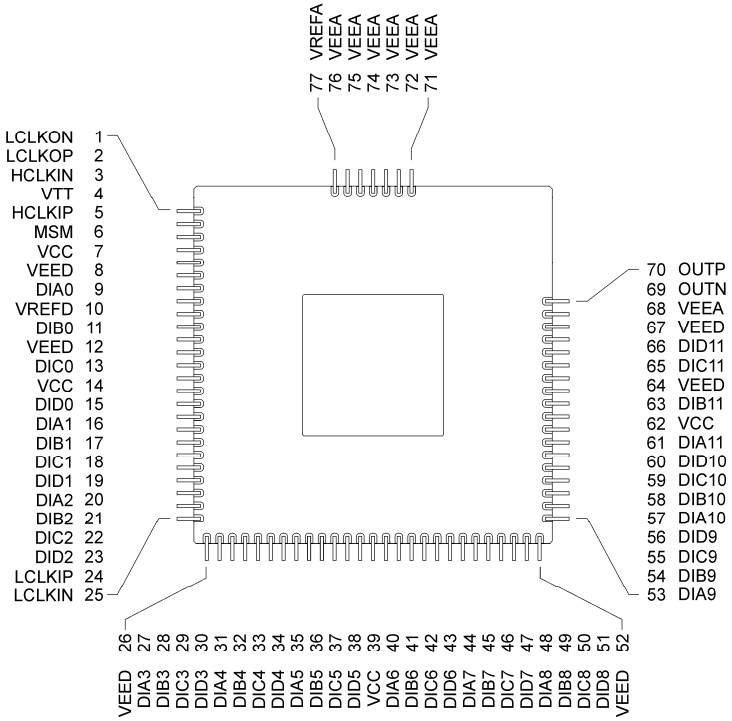

Figure 2 - RDA012M4MS-HD pinout (top view).

Pin Description and Pin Layout (QFP Package)

P/I/O	PIN	NUM.	NAME	FUNCTION
P	41, 62	2	VCC	+3.3V Digital Power Supply
P	2, 3, 6, 7, 8, 9	6	VEEA	-5.2V Analog Power Supply
P	43, 44, 59, 60	4	VEED	-5.2V Digital Power Supply
P	1, 4, 5, 10, 12, 15, 42, 61, 63, 80, 81, 82, 84, 86, 87, 88	16	GND	Ground
P	Bottom Plate	-	GND	Ground
I	11	1	VREFA	-2V Reference Voltage
I	20	1	VREFD	Digital Circuitry Bias Reference. Bypass to Ground
I	17	1	VTT	HCLKI Clock Termination Voltage
I	19	1	MSM	Master-Slave Mode Selection: Float - Master GND - Slave
I	18	1	HCLKIP	Clock Input
I	16	1	HCLKIN	
I	45	1	LCLKIP	Low Clock Input
I	46	1	LCLKIN	
I	14	1	LCLKOP	Low Clock Output
I	13	1	LCLKON	
I	21, 25, 29, 33, 37, 47, 51, 55, 64, 68, 72, 76	12	DIA<0:11>	DIA<i> Is Channel A Digital Bit i Input. MSB is bit 11
I	22, 26, 30, 34, 38, 48, 52, 56, 65, 69, 73, 77	12	DIB<0:11>	DIB<i> Is Channel B Digital Bit i Input. MSB is bit 11
I	23, 27, 31, 35, 39, 49, 53, 57, 66, 70, 74, 78	12	DIC<0:11>	DIC<i> Is Channel C Digital Bit i Input. MSB is bit 11
I	24, 28, 32, 36, 40, 50, 54, 58, 67, 71, 75, 79	12	DID<0:11>	DID<i> Is Channel D Digital Bit i Input. MSB is bit 11
O	85	1	OUTP	Differential Output
O	83	1	OUTN	

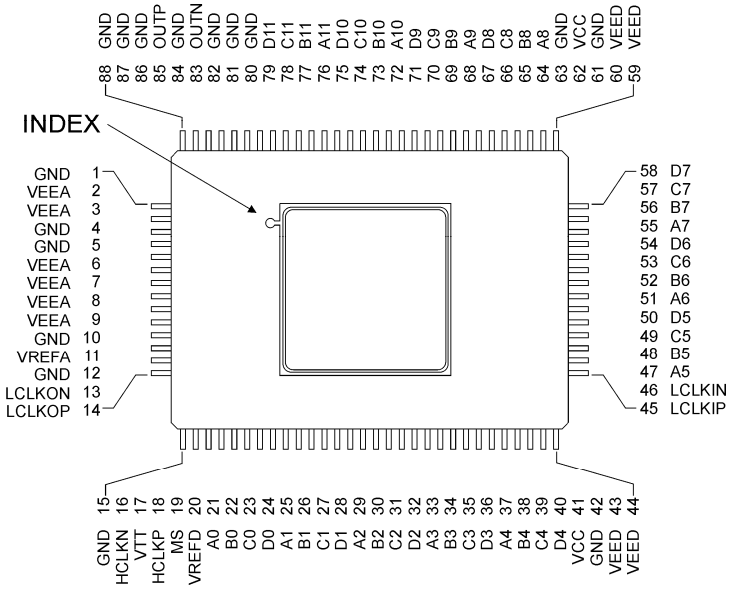

Figure 3 - RDA012M4MS-QP pinout (top view).

The "-QP" products represented in this datasheet are regulated under the International Traffic in Arms Regulations (ITAR)
Public Domain Information – Previously Approved for Public Release (DOD Office of Security Review, Case 08-S-0596)

Pad Layout

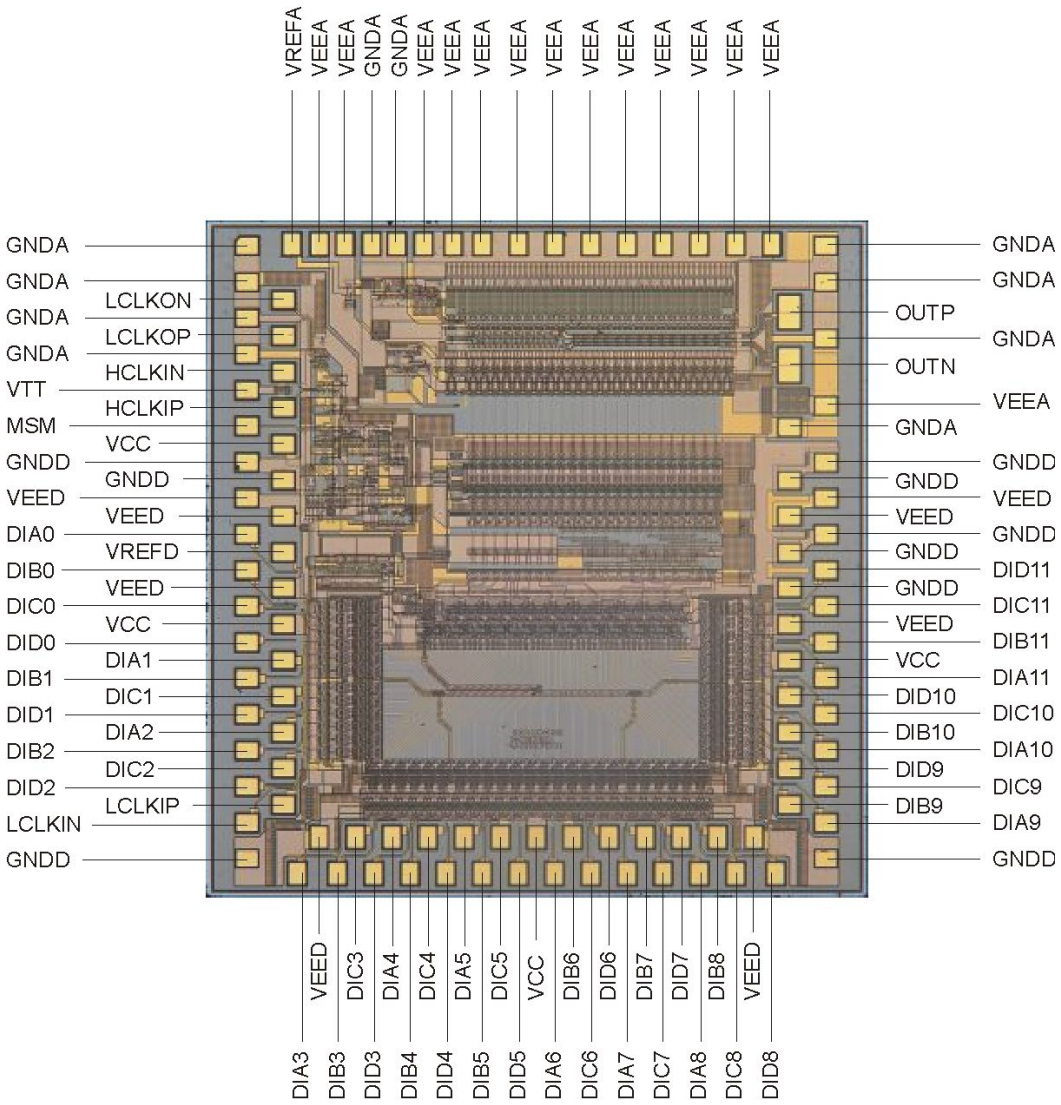

Figure 4 - RDA012M4MS pad layout.

Theory of Operation

For best dynamic and static performance, the DAC employs 6-bit segmentation. The 3.3V NMOS compatible 12-bit digital data inputs are latched by a master-slave flip-flop immediately after the input buffer to reduce the data skew. The four-channel data are combined together by the 48:12 MUX and latched again. The 6 MSB data bits are decoded into thermometer code by a two-stage decoding block, and the 6 LSB data bits are transported through the delay equalizer block. The digital data are synchronized again by a second master slave flip-flop to reduce the switching glitch. The decoded 6 MSB data drive 63 identical current switches, and the 6 LSB data drive 6 current switches. The output nodes from the LSB current switches are connected to the analog output through an R-2R ladder to generate the binary output.

The DAC output full-scale voltage follows the relationship $V_{FS} = 0.3xV_{REF.}$ An internal reference circuit with approximately -10dB supply rejection is integrated on chip for application convenience. The reference pin is provided for monitoring and for bypass purposes. To band-limit the noise on the reference voltage, the reference pin should be bypassed to the GNDA node with capacitance > 100pF. The VREF pin can also be used to override the internal reference with an accurate, temperature-compensated external voltage reference.

The timing diagram is shown in Figure 5. The 1.3GHz external clock (HCLK) is divided by 2 and 4 resulting in the MUX internal selection signals S0 and S1. A low-speed clock (LCLK) is provided to drive the external digital. The four-channel data input are latched with an internal clock that is synchronized with the LCLK. Controlled by S0 and S1, input data are fed to the 1.3GS/s DAC in the order shown.

For applications requiring two MUXDACs, such as quadrature modulation, the RDA012M4MS offers master and slave mode operation. This provides synchronization between the two MUXDACs in a straightforward manner. Figure 7 illustrates two MUXDACs in an I-Q configuration and 1 GS/s conversion rate. The I-MUXDAC is in master mode and the Q-MUXDAC is in slave mode. The master MUXDAC generates an LVDS compatible 250MHz clock signal that is input to the slave MUXDAC where it is used to synchronize the generation of the select signal for the input muxes. The slave device then feeds this clock to the FPGA clock driver. For proper synchronization, the delay associated with the LVDS clock signal from master to slave MUXDAC must not exceed one clock period of the high-speed clock.

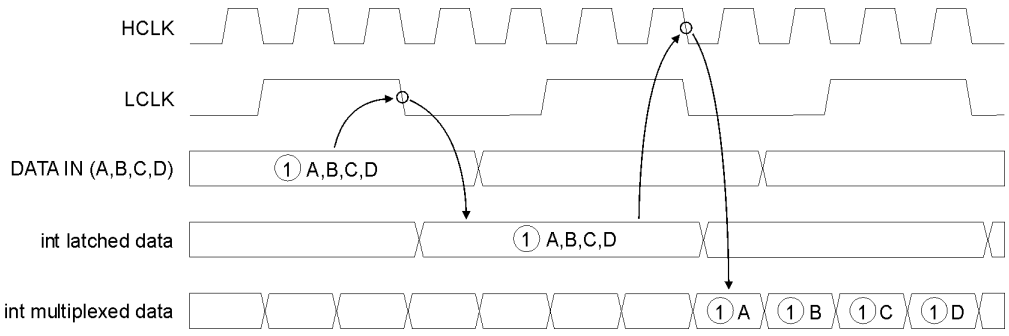

Figure 5 - Input Timing Diagram.

Signal Description

HIGH SPEED INPUT CLOCK.

The RDA012M4MS high-speed clock input is differential and can be driven from typical ECL circuits. Also a differential sinusoidal clock can be used. The HCLKIP and HCLKIN inputs, are internally terminated with 50 Ω to VTT which should be connected to a well decoupled –2.0 volt supply. Since the MUXDAC's output phase noise is directly related to the input clock noise and jitter, a low-jitter clock source is ideal. The internal clock driver generates very little added jitter (~100fs). A 500MHz MUXDAC output demands a white noise induced clock jitter of less than 250fs for a 10-bit equivalent, 62dB SNDR.

DATA INPUT.

The data inputs are 3.3V NMOS-compatible. The data is interleaved according to significant bit. For example, consecutive data pins will occur as A0, B0, C0, D0, A1, B1, etc.

OUTPUT CLOCK.

Output clock LCLKOP and LCLKON are supplied for the DSP/FPGA/ASIC in slave mode, or connected to another MUXDAC if in master mode. They are LVDS compliant and needs to be terminated with a100Ω resistor in front of the clock driver for the ASIC/DSP.

For application convenience, the data input's setup and hold time is specified with respect to the LCLKO. It should be noted that LCLKOP and LCLKON are driven by the MUXDAC and the waveforms of these signals are better defined at the receiver end; that is, near the ASIC/DSP chip that provides the input data for the MUXDAC. The system designer should consider the delay associated with the signal routing in the system's timing budget.

The setup and hold time of the LCLK to data transition are defined at the MUXDAC side. Data transitions of the data input have to occur during the "Valid Data Transition Window." The timing margin seen from the MUXDAC is T_P-T_S where T_P is the LCLKO period and T_S is the setup time, assuming that the ASIC chip takes LCLKO as the clock input and its outputs are latched at the falling edge of the clock. From the ASIC/DSP end, however, the timing margin is decreased by the amount equal to the sum of the data delay and clock delay between the two chips.

ANALOG OUTPUT.

The outputs DACOUTP and DACOUTN should both be connected though a 50 Ω resistor to ground. This will give a full-scale amplitude of 0.6 volt (both outputs must be terminated), 1.2 volt differentially. The output common mode can be changed by terminating the load resistors to a different voltage. The device is optimized to perform best when connected to a voltage between 0 and 1 volt, however. For reliable operation, the output termination voltage should not exceed 3 volts.

REFERENCE.

VREFA is provided for added control of the full-scale amplitude output. The internal reference circuit is designed to provide -2.0 volts, which can change up to ±5% as the supply voltage and/or operating temperature changes. If the user prefers accurate absolute full-scale, use an external voltage reference with low output impedance to override the internal reference. The output full-scale voltage follows the relationship V_{FS} = 0.3xV_{REF}. Note that the MUXDAC is optimized to have the best performance with a reference voltage of -2.0 volts. The output resistance of the reference node is 560 Ω ±10%. VREFD allows adjusting of the digital circuitry bias point for varying input voltage swings. In most cases, VREFD should be bypassed to GND.

Typical Operating Circuit

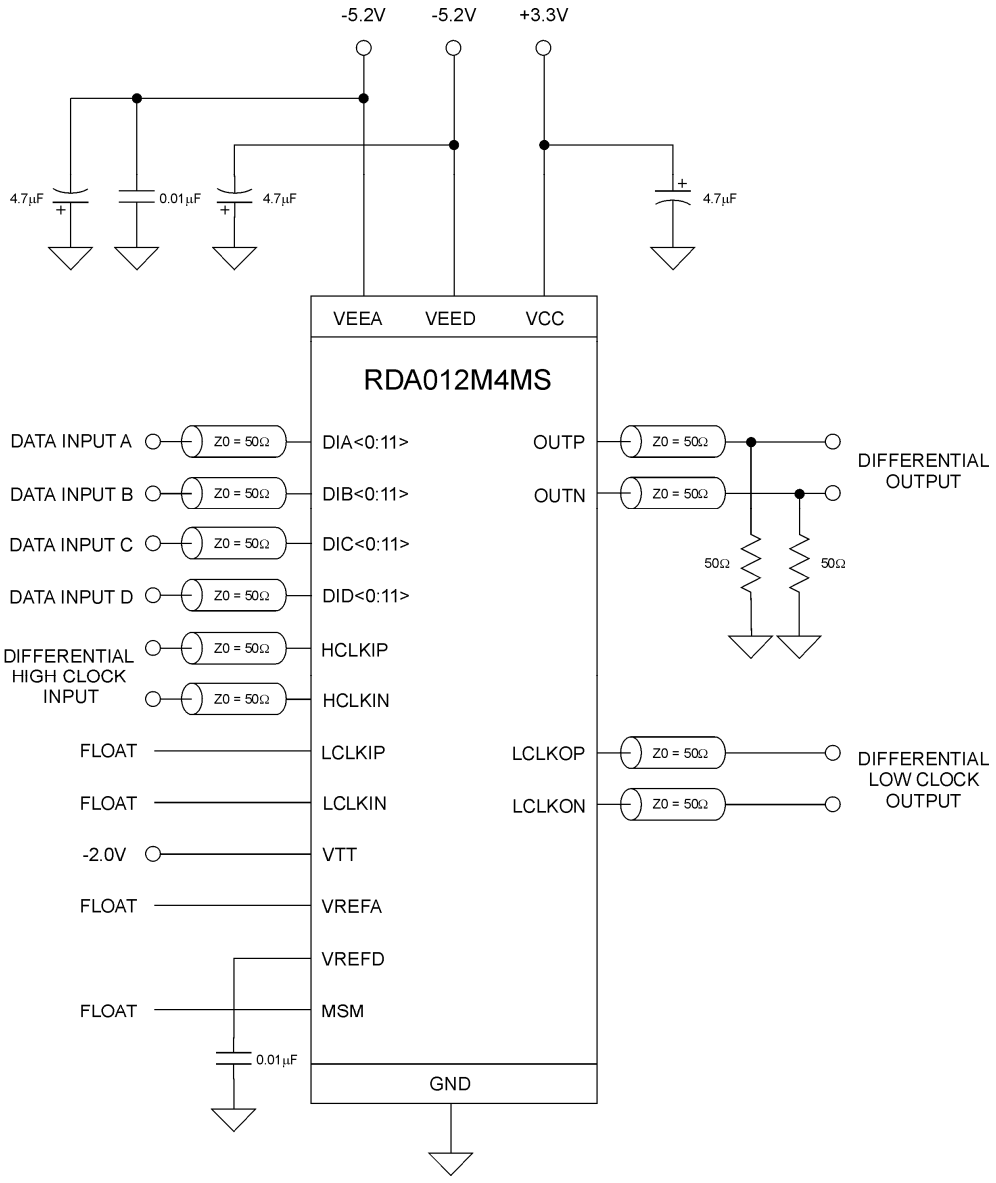

Figure 6 - RDA012M4MS typical operating circuit using the internal voltage reference.

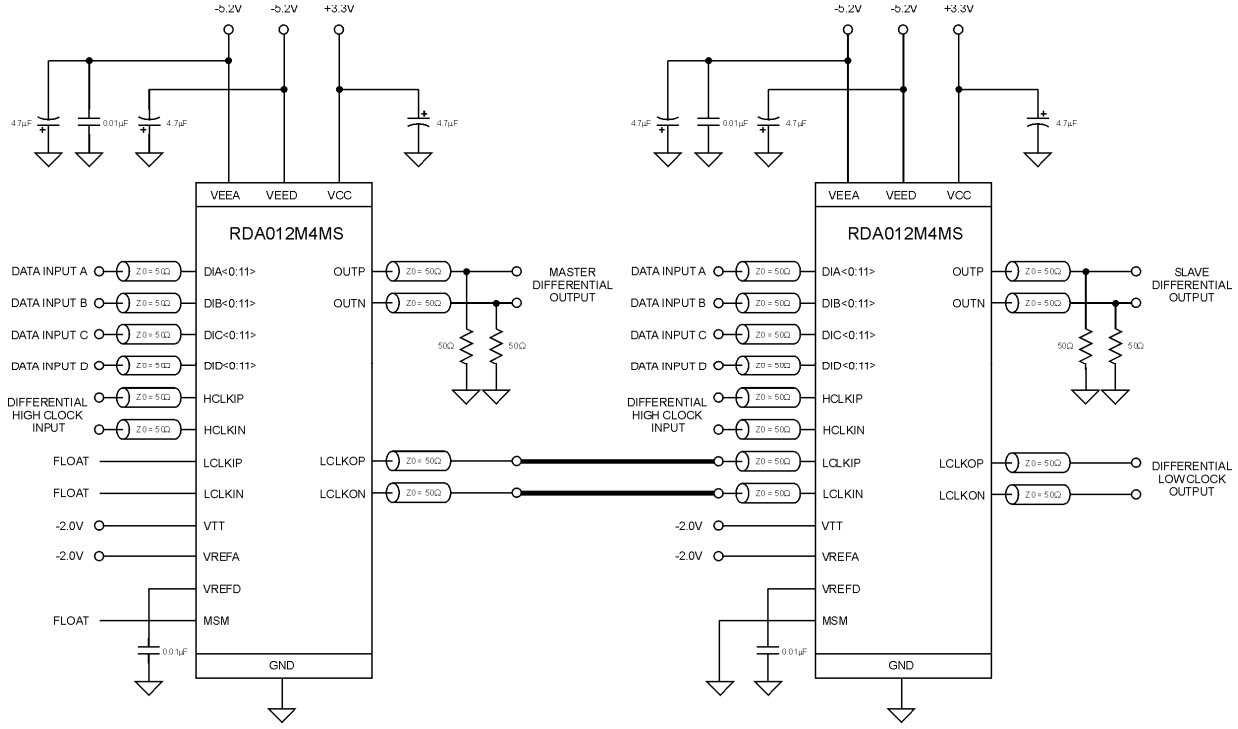

Figure 7 - RDA012M4MS typical operating circuit in master-slave mode using external voltage reference.

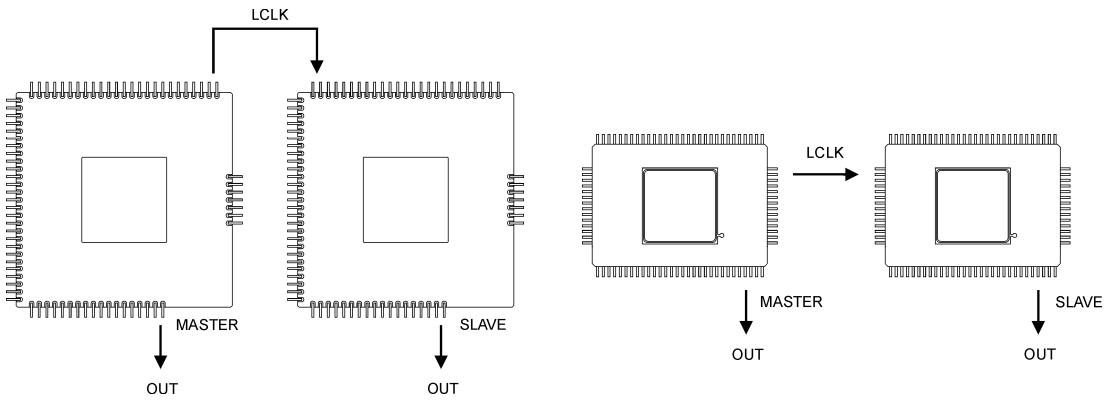

Figure 8 - RDA012M4MS recommended placement in master-slave mode to minimize LCLK routing.

Typical Performance

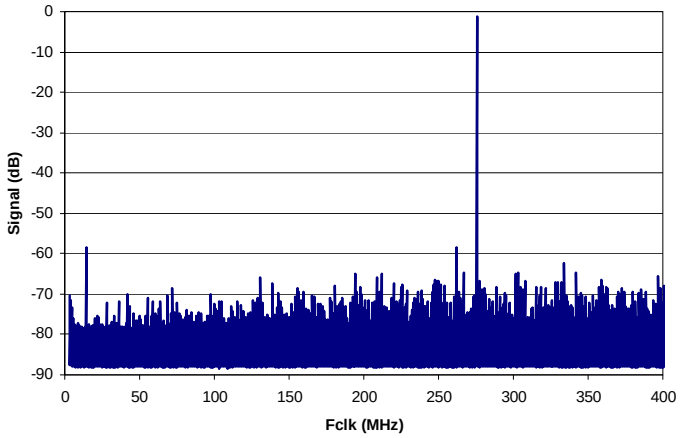

Figure 9 - Output spectrum at Fclk=800MHz, Fout=270MHz

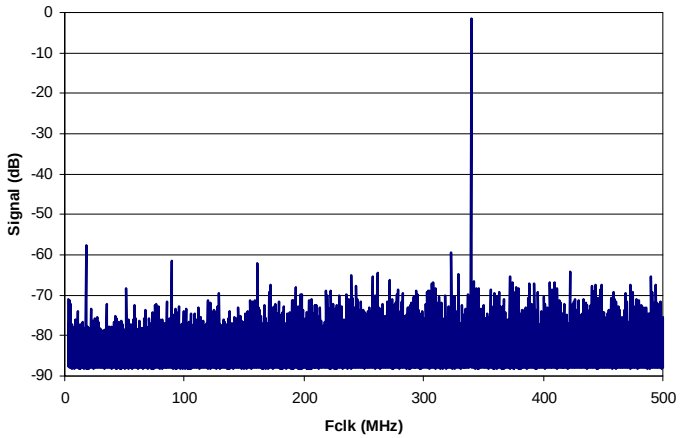

Figure 10 - Output spectrum at Fclk=1000MHz, Fout=340MHz

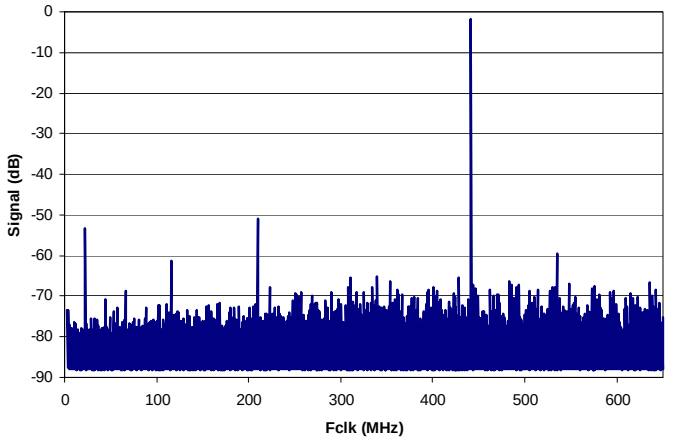

Figure 11 - Output spectrum at Fclk=1300MHz, Fout=440MHz

Package Information – 77 Lead HSD

There is a heat sink slug on the package's bottom. The leads are gull-winged formed and trimmed to 0.053 inch (1.35 mm) in length.

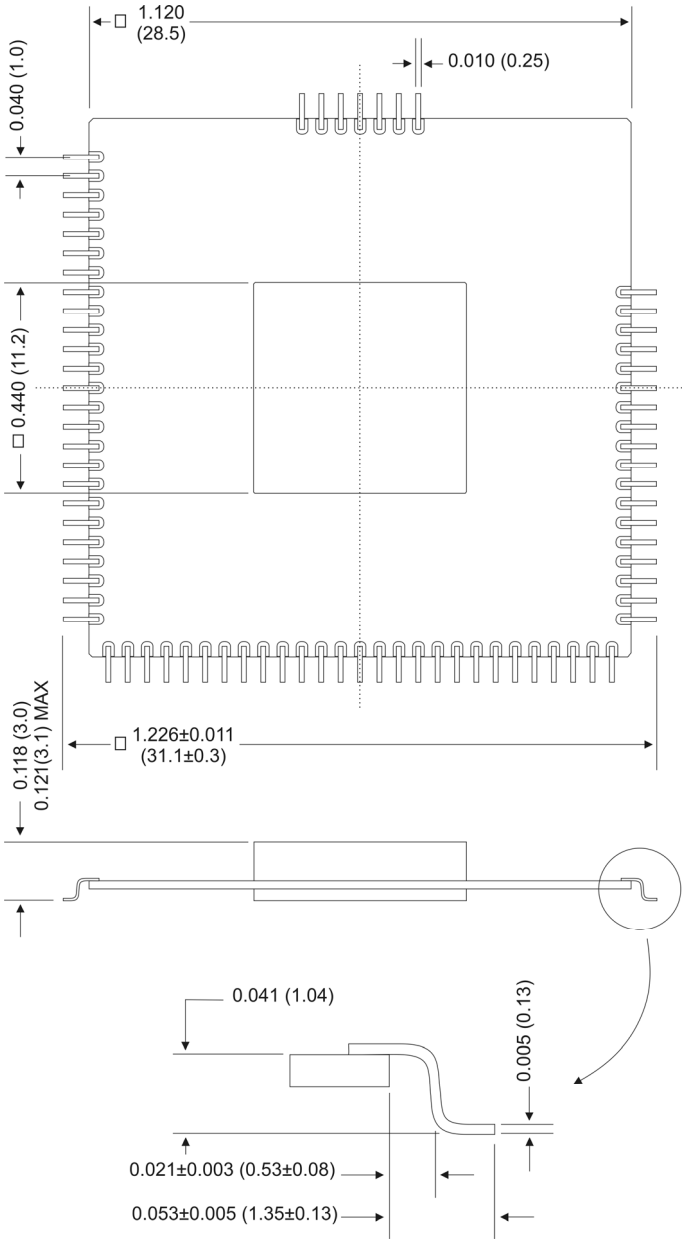

Figure 12 - RDA012M4MS-HD package, dimensions shown in inches (mm).

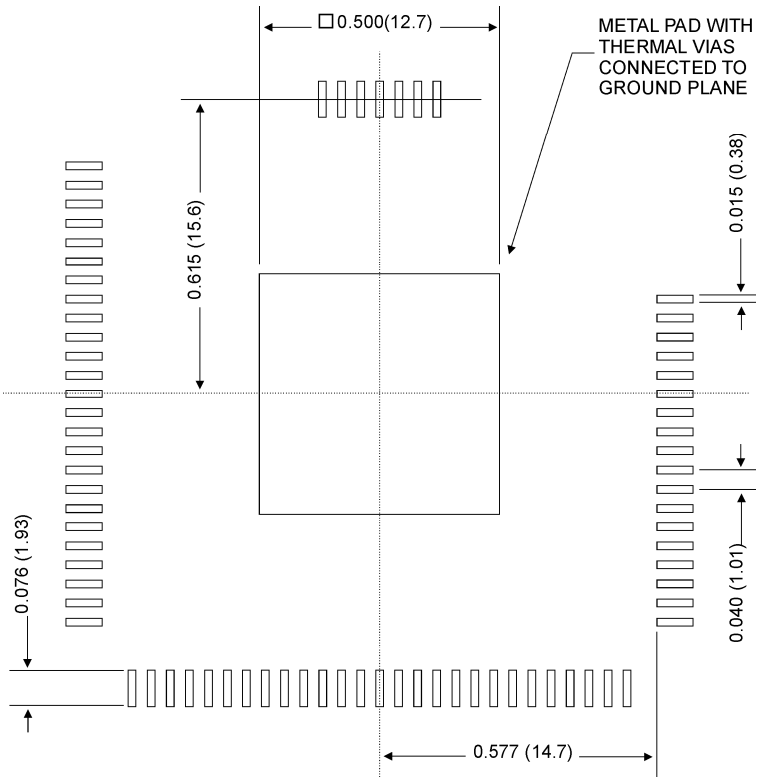

Figure 13 - RDA012M4MS-HD footprint, dimensions shown in inches (mm).

Package Information – 88 Lead QFP

There is a heatsink slug on the package's bottom. The thermal resistance from junction to case (at the heatsink) is approximately 3.5 C/W.

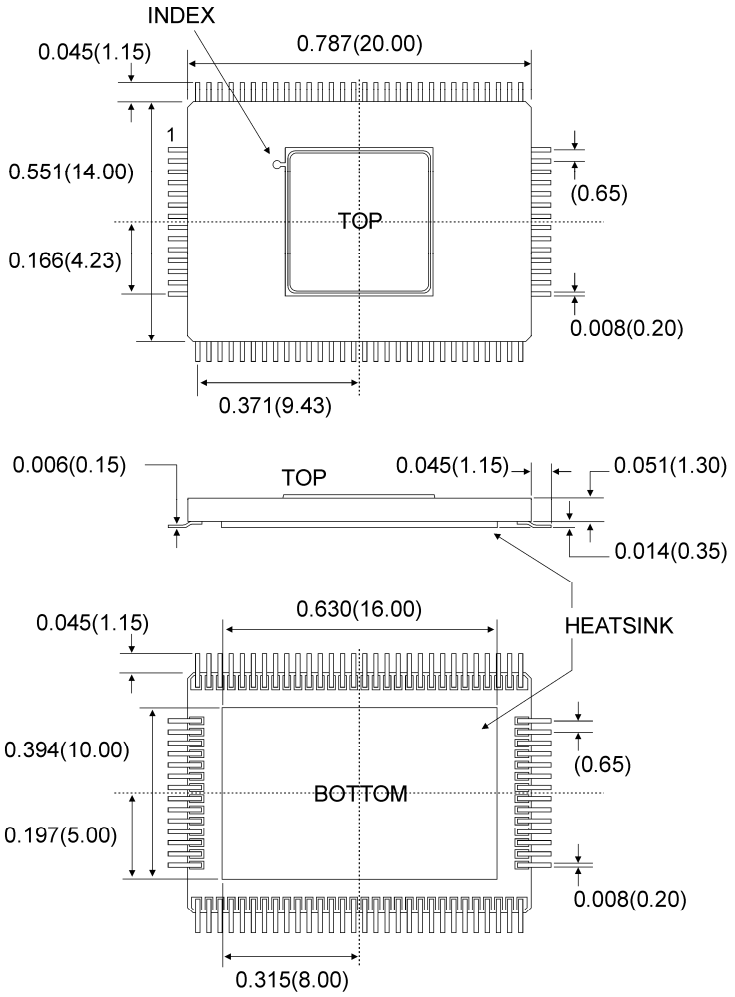

Figure 14 - RDA012M4MS-QP package, dimensions shown in inches (mm).

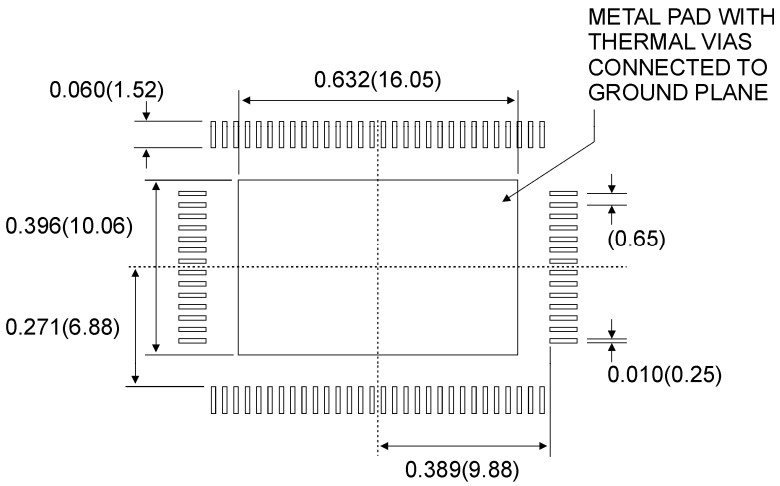

Figure 15 - RDA012M4MS-QP footprint, dimensions shown in inches (mm).