TELEDYNE
SCIENTIFIC COMPANY

RDA112RZ

12 Bit 1.5 GS/s Return to Zero DAC

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12 Bit 1.5 GS/s Return to Zero DAC

Features

- 12 Bit Resolution
- 1.5 GS/s Sampling Rate
- 10 Bit Static Linearity
- LVDS Compliant Digital Inputs
- Power Supply: -5.2V, +3.3V
- Input Code Format: Offset Binary
- Output Swing: 600 mV @ 50 Ω Termination
- Reference I/O Pin for Accurate Full-Scale Adjustment
- Return-to-Zero Output for 2nd Nyquist Operation
- Differential ECL or Sinusoidal Clock Input
- Fast settling time: < 1ns 0.1% (+/- 2LSB), switching from code 1536 to 2560 (quarter scale)

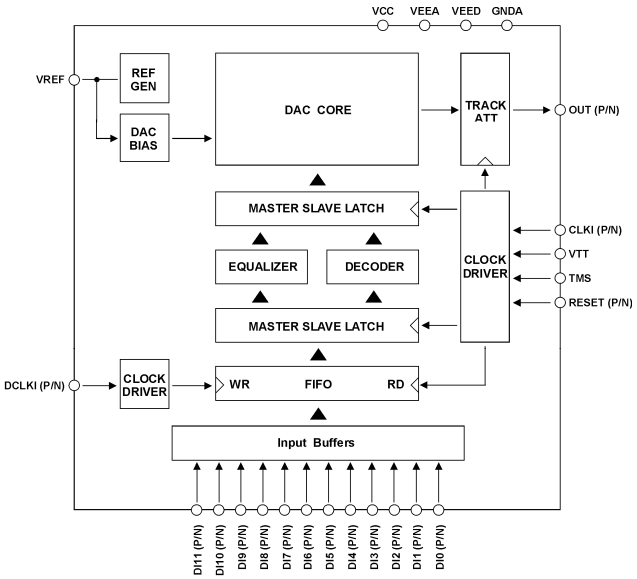

Figure 1 - Functional Block Diagram

Product Description

The RDA112RZ is a GaAs 12 bit digital to analog converter (DAC) with a data sampling rate of 1.5 GS/s. The RDA112RZ has been optimized for applications demanding for a high performance DAC capable of output signal over the 2nd Nyquist band, achieving 60 dBc of spurious free dynamic range (SFDR) at 1.5 GS/s and f_{out} of 667 MHz. The DAC utilizes a segmented current source to reduce glitch energy and achieve high linearity performance. For a flat response at 2nd Nyquist band, a track and attenuate circuit is integrated at the DAC's output.

Ordering information

PART NUMBER	DESCRIPTION
RDA112RZ-QP	12 BIT 1.5GS/s RZDAC, QFP Package
RDA112RZ-DI	12 BIT 1.5GS/s RZDAC, DIE
EVRDA112RZ-QP	RDA112RZ-QP Evaluation Board

CAUTION
DEVICE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)

Absolute Maximum Ratings

Supply Voltages

VEEA, VEED to GNDA ..... -0.3V to +0.3V
VCC to GNDA ..... 0 V to +3.8 V

RF Input Voltages

CLKI to GNDA ..... 0 V to VCCD

HS Digital Input Voltages

DI<11:0> ..... 0 V to VCCD
DCLK ..... 0 V to VCCD
RESET ..... 0 V to VCCD

Temperature

Case Temperature..... -40 to +85 °C
Junction Temperature..... +125 °C
Lead, Soldering (10 Seconds) ..... +220 °C
Storage..... -60 to 125 °C

DC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VCC = 3.3V; VEEA = -5.2V; VEED = -5.2V; VREF = -2V; VTT = -2V; TMS = RZ Mode; Clock: 1.5GHz, 0.6Vpp Differential; Outputs Terminated Into 50 Ω to VCC.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
1.0	**DC TRANSFER FUNCTION**						
1.1	Differential Nonlinearity	DNL		-0.1		0.1	%FS
1.2	Integral Nonlinearity	INL		-0.1		0.1	%FS
2.0	**TEMPERATURE DRIFT**						
2.1	Warm-up Time		After Power-up			30	s
3.0	**CLOCK INPUT (CLKIP, CLKIN)**						
3.1	Input Resistance	R_{CLKI}	Resistance (CLKI P/N) to VTT	45	50	55	Ω
4.0	**DATA CLOCK INPUTS (DCLKIP, DCLKIN)**						
4.1	Input Resistance	R_{DCLKI}	Between P/N Input Pair	90	100	110	Ω
4.2	Input Capacitance	C_{DCLKI}	On Each Input, Single Ended		2		pF
5.0	**DIGITAL INPUTS (DI<0:11>P, DI<0:11>N)**						
5.1	Input Resistance	R_{DIN}	Between P/N Input Pair	90	100	110	Ω
5.2	Input Capacitance	C_{DIN}	On Each Input, Single Ended		2		pF
6.0	**ANALOG OUTPUTS (OUTP, OUTN)**						
6.1	Full-scale Output Swing	V_{FSD}	Differential, Terminated Into 50Ω to GND on Each Output	1140	1200	1260	mVpp
6.2	Full-scale Output Swing	V_{FSS}	Single Ended, Terminated Into 50Ω to GND	570	600	630	mVpp
6.3	Full-scale Output Range	V_{FSRS}	Single Ended, Terminated Into 50Ω to GND (MIN=000h, MAX=FFFh)	-630		0	V
6.4	Output Current	I_{OUT}	Terminated Into 50Ω to GND	11.4	12	12.6	mA
7.0	**REFERENCE (VREF)**						
7.1	Reference Voltage	V_{VREF}			-2		V
8.0	**POWER SUPPLY REQUIREMENTS**						
8.1	Positive Current	ICC			45		mA
8.2	Negative Current, Analog	IEEA			120		mA
8.3	Negative Current, Digital	IEED			400		mA
8.4	Power Dissipation	P			2.8	3.1	W

AC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VCC = 3.3V; VEEA = -5.2V; VEED = -5.2V; VREF = -2V; VTT = -2V; TMS = RZ Mode; Clock: 1.5GHz, 0.6Vpp Differential; Outputs Terminated Into 50 Ω to VCC.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
9.0	**DYNAMIC PERFORMANCE**						
9.1	Spurious Free Dynamic Range	SFDR1	F_{clk} = 1500MHz , F_{out} = 825MHz		55		dBc
9.2		SFDR2	F_{clk} = 1500MHz , F_{out} = 995MHz		58		dBc
9.3		SFDR3	F_{clk} = 1500MHz , F_{out} = 1090MHz		54		dBc
9.4		SFDR4	F_{clk} = 1500MHz , F_{out} = 1450MHz		56		dBc
9.5	Clock Feedthrough	FD	F_{clk} = 1000MHz			-40	dB
9.6	Output Flatness	ATT	Attenuation at F_{out} = 950MHz			6	dB

Operating Conditions

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
10.0	**CLOCK INPUTS (CLKIP, CLKIN)**						
10.1	Amplitude	$V_{CPP,HCLKI}$	Differential	400	600	800	mV
10.2	Common Mode Voltage	$V_{CCM,HCLKI}$		-2	-1.5	-0.8	V
10.3	Maximum Frequency	$F_{MAX,HCLKI}$		1500			MHz
10.4	Minimum Frequency	$F_{MIN,HCLKI}$				1	MHz
11.0	**DATA CLOCK INPUTS (DCLKIP, DCLKIN)**						
11.1	Amplitude	V_{DPP}	Differential	200			mV
11.2	Common Mode Voltage	V_{DCM}		0.2		2.2	V
12.0	**DIGITAL INPUTS (DI<0:11>P, DI<0:11>N)**						
12.1	Amplitude	V_{DPP}	Differential	200			mV
12.2	Common Mode Voltage	V_{DCM}		0.2		2.2	V
12.3	Data In to DCLKI Setup	t_{DTDKST}	Both Edges of DCLKI	100			ps
12.4	Data In to DCLKI Hold	t_{DTDKHD}	Both Edges of DCLKI	100			ps
13.0	**TERMINATION VOLTAGE (VTT)**						
13.1	Reference Voltage	V_{TT}	Termination Voltage for CLKI		-2		V
14.0	**REFERENCE (VREF)**						
14.1	Reference Voltage	V_{REF}	External Reference		-2		V
15.0	**POWER SUPPLY REQUIREMENTS**						
15.1	Positive Supply	VCC		3.1	3.3	3.5	V
15.2	Negative Supply, Analog	VEEA		-5.45	-5.2	-4.75	V
15.3	Negative Supply, Digital	VEED		-5.45	-5.2	-4.75	V
16.0	**OPERATING TEMPERATURE**						
16.1	Case Temperature	Tc	Measured at Bottom Plate	-40		85	°C
16.2	Junction Temperature	Tj				125	°C

Pin Description

P/I/O	PIN	NUM.	NAME	FUNCTION
P	23	1	VCC	VCC Power Supply
P	48, 53, 54, 55, 56, 57, 58	7	VEEA	Analog VEE Power Supply
P	2, 15, 24, 32, 41	5	VEED	Digital VEE Power Supply
P	1, 4, 16, 31, 39, 42, 47, 50, 52, 59, bottom plate	10	GND	Ground
I	3	1	VRD1	Test Pin: Bypass to Ground
I	40	1	VRD2	Test Pin: Bypass to Ground
I	60	1	VREF	-2V External Reference Voltage
I	44	1	VTT	Clock Termination Voltage
I	46	1	TMS	Track Mode Select: Float – RZ Function Ground – ZOH Function
I	19	1	RESETP	RESETP / RESETN Is Reset Input
I	20	1	RESETN	
I	45	1	CLKIP	CLKIP / CLKIN Is Clock Input
I	43	1	CLKIN	
I	5, 7, 9, 11, 13, 17, 25, 27, 29, 33, 35, 37	1	DI<I>P	DI<I>P / DI<I>N Is Digital Bit I Input. MSB is Bit 11.
I	6, 8, 10, 12, 14, 18, 26, 28, 30, 34, 36, 38	1	DI<I>N	
I	21	1	DCLKIP	DCLKIP / DCLKIN Is Data Clock Input
I	22	1	DCLKIN	
O	51	1	OUTP	OUTP / OUTN Is Differential Output
O	49	1	OUTN	

Pin Layout (TOP view)

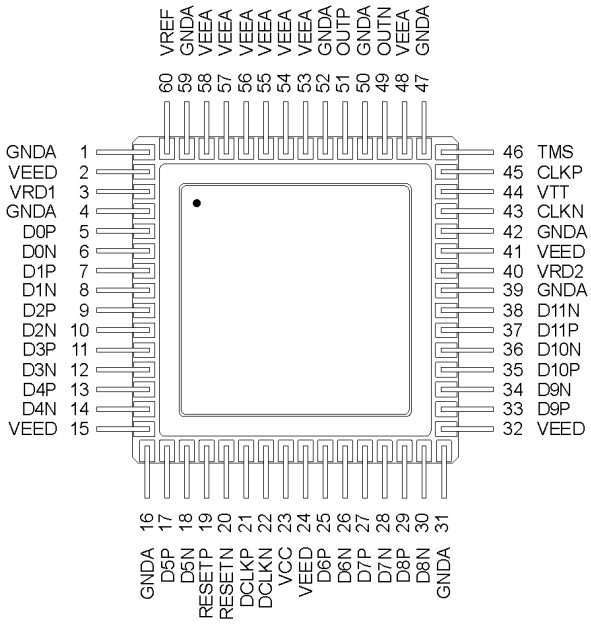

Figure 2 - RDA112RZ-QP pinout (top view).

Die Plot and Pad Arrangement

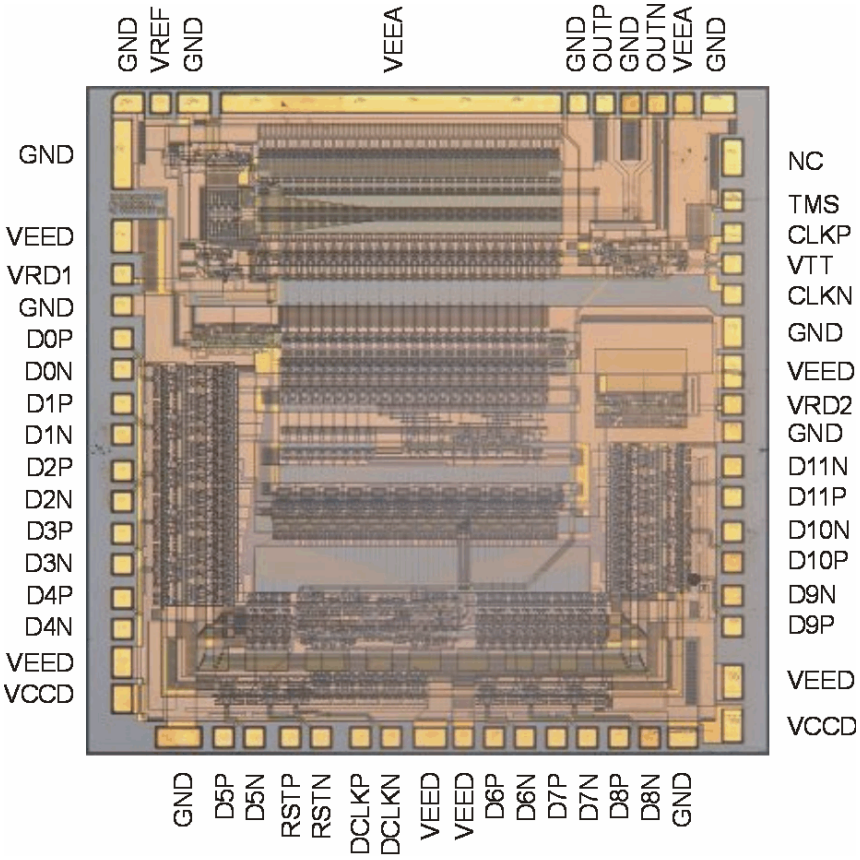

Figure 3 – RDA112RZ die pad layout.

Typical Operating Circuit

The DAC employs MSB segmentation, and the number of bits segmented is carefully chosen for the best compromise between static and dynamic linearity. The 12-bit digital data inputs are latched by a master-slave flip-flop immediately after the input buffer to reduce data skew. MSB data bits are decoded into a thermometer code by a two-stage decoding block, and the LSB data bits are transported through the delay equalizer block. The digital data are synchronized again by a second master-slave flip-flop to reduce the switching glitch. The decoded MSB and LSB data bits drive identical current switches. The output nodes from the LSB current switches are connected to the analog output through a R-2R ladder to generate the binary-weighted analog output.

A track-and-attenuator (T/A) circuit is integrated with the DAC, for a wider output bandwidth. A traditional DAC can be modeled as an ideal sampler followed by a zero order hold (ZOH) circuit to the DAC. Due to the sinc(x) (=sin(x)/x) frequency behavior of the ZOH circuit, the DAC output has notches at the frequencies which are multiples of the sampling clock frequency. Also, the DAC's glitch causes unwanted spurious tones when the output frequency of the DAC is high. A track-and-hold amplifier can be used to re-sample the DAC output, mainly to reduce the performance degradation due to the glitch caused by the different switching instances of the DAC current switches. A carefully designed track-and-hold successfully de-glitches the DAC output, but the signal drop due to the sinc(x) characteristics still remains. The spectral flatness of the DAC output can be improved by implementing return-to-zero (RZ) DAC. The RZ DAC output can be achieved by adding a track-and-attenuator circuit after the DAC. For an RZ DAC with an output duty cycle of D, the DC output power loss is $-20*\log_{10}(D)$, but the output notch happens at multiples of Fclk/D. For example when the duty cycle is 50% the notch is at 3GHz, 6GHz, etc for a 1.5GS/s RZ DAC. The T/A circuit add spurs of its own.

The DAC output full-scale voltage follows the relationship $V_{FS} = 0.3xV_{REF.}$ An internal reference circuit with approximately 20dB supply rejection is integrated on chip for a convenient application, and a reference pin is provided for monitoring and for bypass purposes. To band-limit the noise on the reference voltage, the reference pin should be bypassed to the GNDA node with capacitance > 100pF. The VREF pin can also be used to override the internal reference with an accurate, temperature-compensated external voltage reference. **Error! Reference source not found.** shows the equivalent circuit of the DAC output ports. The DAC outputs are terminated internally to GNDA with 50Ω equivalent resistors, and need an external 50 termination to at the output pin for a full-scale voltage of 600mV with a 2-volt reference voltage.

A 4-clock deep FIFO is included to compensate the delay skews in the data and clock line. The incoming digital data is latched on both edges of the DCLK. As a result, for 1.5Gb/s data stream, the input DCLK will have 750MHz frequency, so that the clock shape will be similar to the data signal except that the DCLK waveform would be shifted by 90°. In other words, the rising and falling edges of the DCLK will happen at the moment that the data signals have the widest windows to latch onto. The read clock of the FIFO will start reading the incoming data after the RESET is set to logic 0.

Signal Description

POWER SUPPLIES

The RDA112RZ has several power supplies. Their names and uses are defined in the pin description section. Different power supply pins are separated inside the chip, and using separate regulators for each supply is recommended for a good isolation between the digital and analog sections of the chip. No power sequencing is required for reliable operation. Also due to the high-breakdown voltage of the device technology, input may be activated upon an unpowered DAC without damaging the part.

ANALOG OUTPUT and REFERENCE

The outputs OUTP and OUTN should both be connected though a 50 Ω resistor to GNDA. This will give a full-scale amplitude of 0.6 volt, 1.2-volt differentially.

VREF pin is provided for an added control over the full-scale of the DAC. The internal reference circuit is designed to provide -2.0 volt with –20dB VEE power supply sensitivity (PSS), which can change up to ±5% as the supply voltage and/or operating temperature changes. If the user prefers accurate absolute full-scale, one can use external voltage reference with low output impedance to override the internal reference. Separate reference pins are provided for the digital reference voltage as well. However the accuracy of the digital reference voltages are not as crucial as the analog reference. A proper bypass circuitry would suffice for the digital reference pins. Note that the DAC is designed for a reference voltage of -2.0 volt. The output resistance of the reference node is 560 Ω ±10%.

INPUT CLOCK

The RDA112RZ clock inputs can be driven from a typical ECL circuits. Also a differential sinusoidal clock can be used to drive the DAC. A differential clock should be provided to the CLKP and CLKN inputs, which are internally terminated with 50Ω. The VTT pin is the termination node for both CLKP and CLKN, and should be connected to a well de-coupled –2.0 volt supply. Since the DAC's output phase noise is directly related to the input clock noise and jitter, a low-jitter clock source should be used to drive the clock input. The internal clock driver generates very little added jitter (~100fs) to the internal clock, and the incoming clock signal's spectral purity needs to be guaranteed to take advantage of the low-noise clock driver circuit inside. A 900MHz DAC output demands a white-noise induced clock jitter of less than 280fs for a 10-bit equivalent, 62dB SNR.

DATA INPUT and DCLOCK

According to the LVDS standards, data inputs need to have 100 Ω terminations between the positive and the complimentary terminals. For convenient application and better performance, the termination resistors are included on the chip.

The data input clock is supplied by the DSP or ASIC that provides the digital data for the DAC. RDA112RZ employs a four (4)-clock deep FIFO to provide a robust interfacing with the digital driver chip. The digital data are written to the FIFO on both edges of the DCLK, and read into the DAC register on each rising edge of the DAC clock (CLKI). A four-clock deep FIFO provides a skew margin of worst-case 1½ full clock cycle in both positive and negative direction. To ensure a robust data interface, RESET pin is provided. The read clock of the FIFO is enabled when RESET signal is low, starts to feed the digital data to the DAC.

A timing example scenario is given in **Error! Reference source not found.**. When the RESET signal goes low, the data stored in the register FIFO1 exhibits the widest timing window. So the data D(1) is taken into the F/F from the FIFO. By employing 4 clock deep FIFO, maximum delay fluctuation of 1.5 t_{ck} between the RCLK and the DCLK can be tolerated.

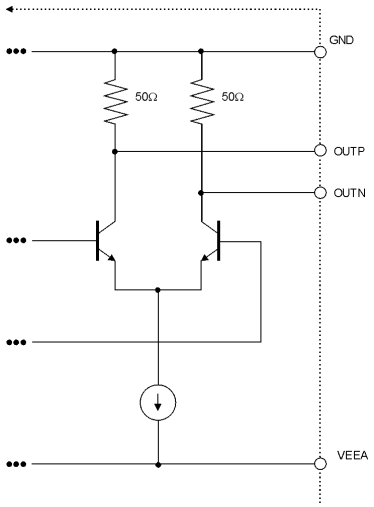

Figure 4 – RDA112RZ equivalent output circuit.

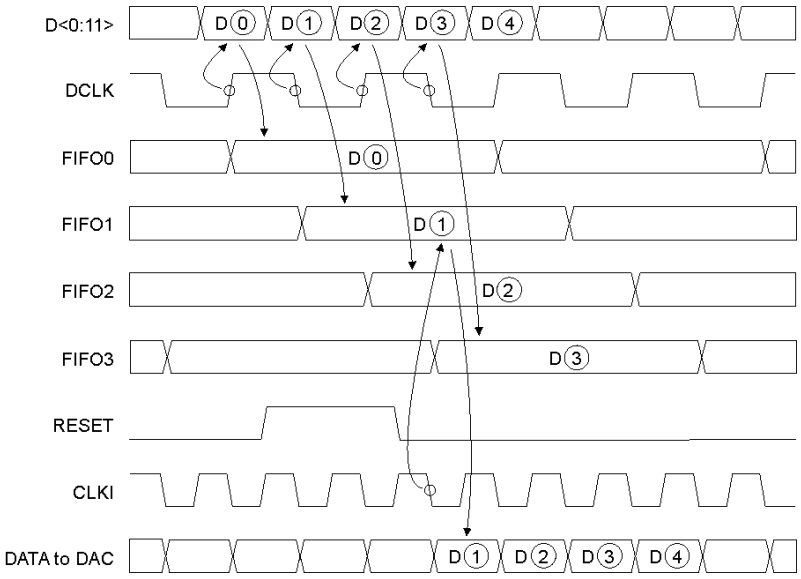

Figure 5 – RDA112RZ input data timing.

Typical Operating Circuit

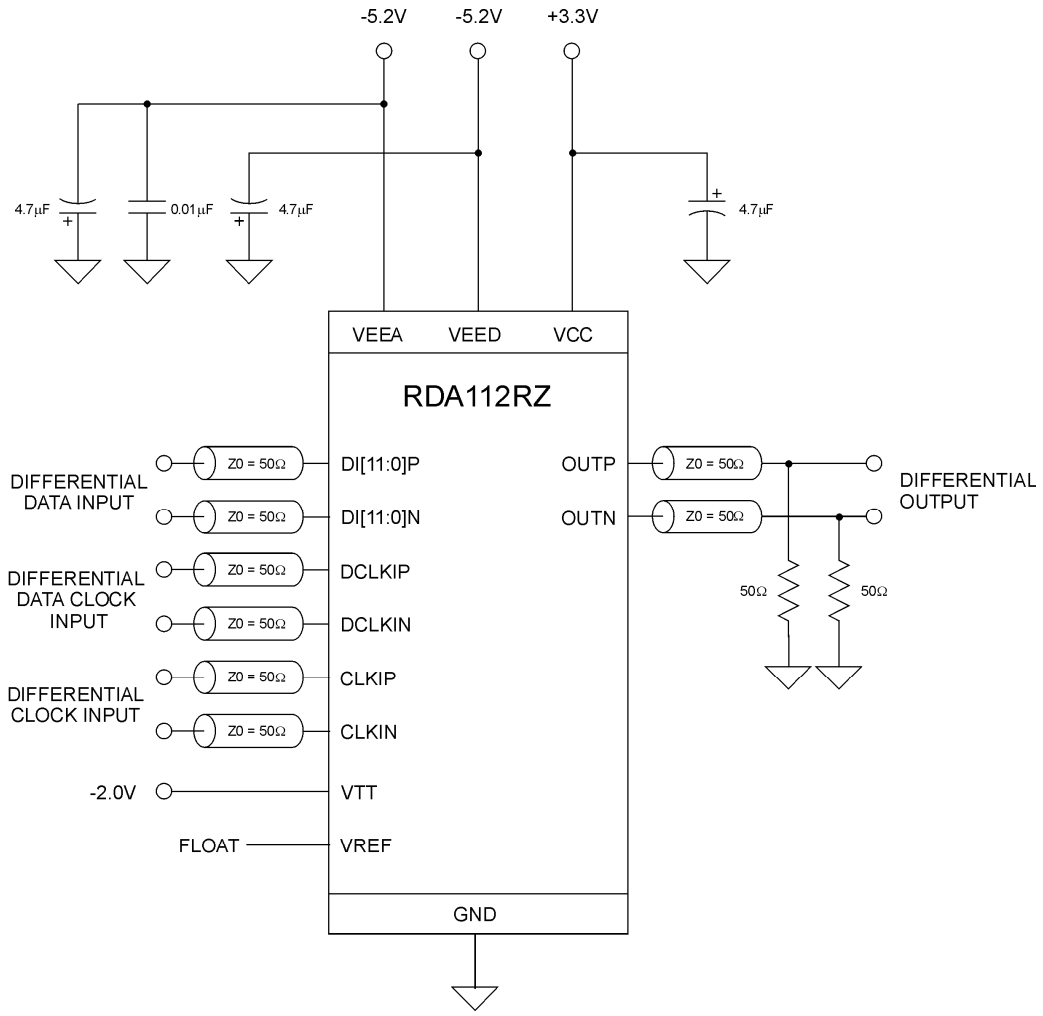

Figure 6 - RDA112RZ typical operating circuit using internal voltage reference.

Package Information

The RDA112RZ is shipped in a 60-pin QFP. The package has a CuW base for heat spreading that should be soldered to copper on a PCB. The Package body including lid is electrically tied to GND internally. All dimensions are in inches (mm). Tolerances are ±0.005 inches, unless otherwise noted.

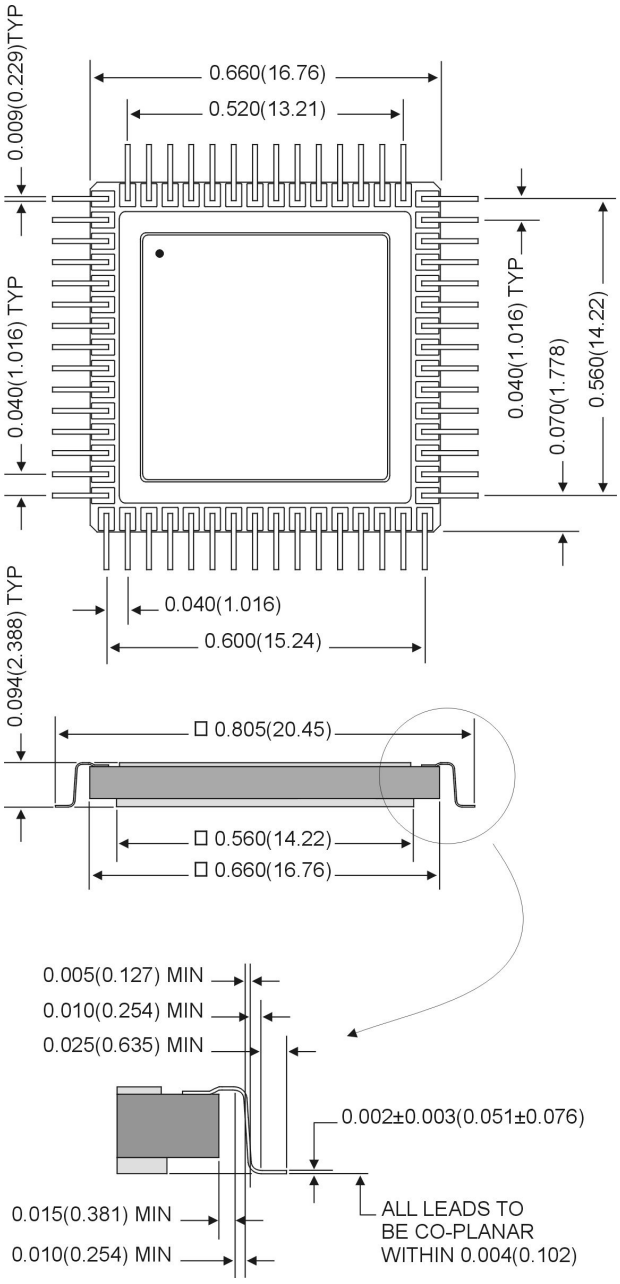

Figure 7 - RDA112RZ-QP package, dimensions shown in inches (mm).