TELEDYNE
SCIENTIFIC COMPANY

RTH050

15 GHz Bandwidth 1 GS/s Dual Track-and-Hold

REV-DATE PA4-2412
FILE DS_0082PA4-2412

DS

RTH050

15 GHz Bandwidth 1 GS/s Dual Track-and-Hold

Features

- 15 GHz Small Signal Input Bandwidth
- 13 GHz Input Bandwidth (0.25 Vpp SE)
- 100 - 1000 MHz Sampling Rate (TH1)
- 10 - 1000 MHz Output Data Rate (TH2)
- -40 dB Hold Mode Distortion (4.0 GHz 0.25 Vpp SE V_{IN})
- -36 dB Hold Mode Distortion (4.0 GHz 0.25 Vpp SE V_{IN})
- < 50 fs Aperture Jitter
- < 200 ps Acquisition Time
- < 25 ps Rise Time (20 - 80%)
- Differential Analog Input/Output
- 1.6W Power Dissipation
- Output Held more than Half Clock Cycle
- Track Mode Select*
- RoHS Compliant** ***

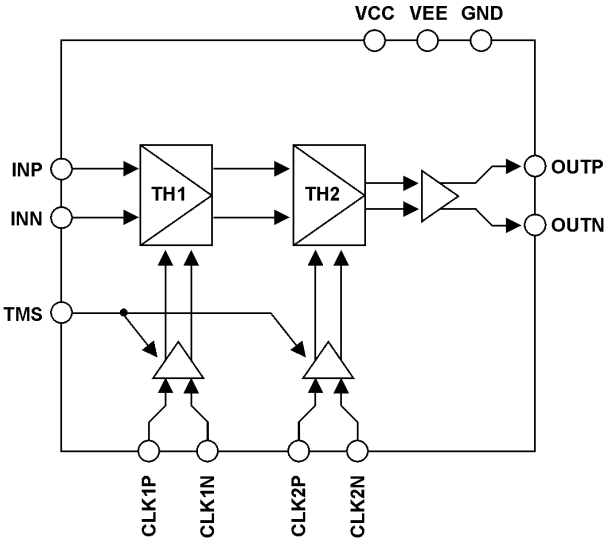

Figure 1 - Functional Block Diagram

Product Description

RTH050's bandwidth and aperture jitter enable 1 GS/s accurate sampling of DC to multi-GHz signals. The differential-to-differential dual track-and-hold cascades two track-and-hold circuits, TH1 and TH2. The RTH050 provides a held output for more than half a clock cycle, easing bandwidth requirements of subsequent circuitry relative to the case of a single track-and-hold (TH). The option to independently clock TH1 and TH2 (as low as 10 MHz) further relaxes this requirement for sub-sampling applications.

Ordering information

PART NUMBER	DESCRIPTION
RTH050-BG	49 Ball BGA Package
RTH050-HD	13 Lead HSD Package (RoHS)
RTH050-HQ	24 Lead QFP Package (RoHS)
RTH050-DI	Die
EVRTH050-HD	Evaluation Board with a RTH050-HD

CAUTION
DEVICE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)

* Not available in the RTH050-BG
** The RTH050-HD, RTH050-HQ are RoHS compliant.
*** Please contact us for price and availability for a RoHS version of the RTH050-BG.

Absolute Maximum Ratings

Supply Voltages

VCC to GND ..... -1 to +6 V
VEE to GND ..... -6 to +1 V
VCC to VEE .....-1 to +11 V

Input Voltages

INP, INN to GND .....-1 to +1 V
CLK1P, CLK1N, CLK2P, CLK2N to GND ..... -1 to +1 V
TMS to GND ..... -6 to +1 V

Output Voltages

Vterm (Output Termination Voltage) to GND.. -2.5 to +0.5V

Temperature

Case Temperature ..... -15 to +85 °C
Junction Temperature ..... +125 °C
Lead, Soldering (10 Seconds) ..... +220 °C
Storage ..... -40 to 125 °C

DC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VCC = 5V; VEE = -5.2V; Clocks: 1GHz, 0.6Vpp Differential; Input: 250mV Single-Ended; Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
1.0	**DC TRANSFER FUNCTION**						
1.1	Gain	G		-3.0		-2.3	dB
1.2	Offset Voltage	V_{OFF}	Absolute Value			18	mV
1.3	Common-Mode Rejection	CMRR	0.25 Vpp at INP and INN, in phase		-60		dB
2.0	**TEMPERATURE DRIFT**						
2.1	Warm-up Time		After Power-up			10	s
2.2	Gain Drift		After Warm-up, from 20°C to 120°C		740		ppm/°C
2.3	Offset Voltage Drift		After Warm-up, from 20°C to 120°C		7		µV/°C
2.4	Offset Voltage Drift					±340	µV/yr
3.0	**ANALOG INPUT (INP, INN)**						
3.1	Input Resistance	R_{IIN}	Each Lead to GND	46	50	54	Ω
3.2	Input Capacitance	C_{IIN}	Each Lead to GND			300	fF
4.0	**CLOCK INPUTS (CLK1P, CLK1N, CLK2P, CLK2N)**						
4.1	Input Resistance	R_{CIN}	Each Lead to GND	46	50	54	Ω
4.2	Input Capacitance	C_{CIN}	Each Lead to GND			300	fF
5.0	**DIGITAL INPUT (TMS)**						
5.1	Current Draw		Into Lead, High		0.75		mA
6.0	**ANALOG OUTPUT (OUTP, OUTN)**						
6.1	Common Mode Voltage	OUT_{CM}	Relative to Vterm	-0.7	-0.6	-0.5	V
6.2	Average Current		Into Each Output Lead		12		mA
6.3	Maximum Current		Into Output Lead		20		mA
7.0	**POWER SUPPLY REQUIREMENTS**						
7.1	Positive Supply Current	ICC			80		mA
7.2	Negative Supply Current	IEE			230		mA
7.3	Power Dissipation	P			1.6	1.9	W

AC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VCC = 5V; VEE = -5.2V; Clocks: 1GHz, 0.6Vpp Differential; Input: 250mV Single-Ended; Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
8.0	**DYNAMIC TRACK MODE PERFORMANCE, SINEWAVE INPUT**						
8.1	Track Bandwidth		-3dB Gain, TH1 & TH2 In Track Mode		1000		MHz
8.2	Gain Flatness Deviation					±0.5	dB
8.3	Integrated Noise		Input Referred		800		μV
8.4	Noise Floor		Input Referred		6.7		nV/√Hz
9.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT**						
9.1	Gain Flatness Deviation	GFD	From DC to 6GHz			±1	dB
9.2	Integrated Noise		Input Referred		1600		μV
9.3	Noise Floor		Input Referred		10		nV/√Hz
10.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.125Vpp SINGLE ENDED**						
10.1	Bandwidth	BW_L	-3dB Gain, 0.125 V_{PP} Single Ended Input	15	16		GHz
10.2	SFDR 60 MHz	SFDR1	0.125 Vpp Single Ended Input	62	66		dB
10.3	SFDR 1060 MHz	SFDR2	0.125 Vpp Single Ended Input	57	62		dB
10.4	SFDR 2060 MHz	SFDR3	0.125 Vpp Single Ended Input	46	50		dB
10.5	SFDR 3060 MHz	SFDR4	0.125 Vpp Single Ended Input	39	41		dB
10.6	SFDR 4060 MHz	SFDR5	0.125 Vpp Single Ended Input	38	40		dB
10.7	SFDR 5060 MHz	SFDR6	0.125 Vpp Single Ended Input	34	36		dB
10.8	SFDR 6060 MHz	SFDR7	0.125 Vpp Single Ended Input	31	33		dB
10.9	SFDR 7060 MHz	SFDR8	0.125 Vpp Single Ended Input	29	31		dB
10.10	SFDR 8060 MHz	SFDR9	0.125 Vpp Single Ended Input	27	29		dB
10.11	SFDR 9060 MHz	SFDR10	0.125 Vpp Single Ended Input	25	26		dB
10.12	SFDR 10060 MHz	SFDR11	0.125 Vpp Single Ended Input	26	27		dB
10.13	SFDR 11060 MHz	SFDR12	0.125 Vpp Single Ended Input	27	28		dB
10.14	SFDR 12060 MHz	SFDR13	0.125 Vpp Single Ended Input	25	28		dB
10.15	THD 60 MHz	THD1	0.125 Vpp Single Ended Input		-65	-62	dB
10.16	THD 1060 MHz	THD2	0.125 Vpp Single Ended Input		-61	-57	dB
10.17	THD 2060 MHz	THD3	0.125 Vpp Single Ended Input		-50	-45	dB
10.18	THD 3060 MHz	THD4	0.125 Vpp Single Ended Input		-41	-39	dB
10.19	THD 4060 MHz	THD5	0.125 Vpp Single Ended Input		-40	-38	dB
10.20	THD 5060 MHz	THD6	0.125 Vpp Single Ended Input		-36	-34	dB
10.21	THD 6060 MHz	THD7	0.125 Vpp Single Ended Input		-33	-31	dB
10.22	THD 7060 MHz	THD8	0.125 Vpp Single Ended Input		-31	-29	dB
10.23	THD 8060 MHz	THD9	0.125 Vpp Single Ended Input		-28	-27	dB
10.24	THD 9060 MHz	THD10	0.125 Vpp Single Ended Input		-26	-24	dB
10.25	THD 10060 MHz	THD11	0.125 Vpp Single Ended Input		-27	-26	dB
10.26	THD 11060 MHz	THD12	0.125 Vpp Single Ended Input		-28	-27	dB
10.27	THD 12060 MHz	THD13	0.125 Vpp Single Ended Input		-28	-25	dB

Test Conditions (see notes for specific conditions): Room Temperature; VCC = 5V; VEE = -5.2V; Clocks: 1GHz, 0.6Vpp Differential; Input: 250mV Single-Ended; Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
11.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.25Vpp SINGLE ENDED**						
11.1	Bandwidth	BW_M	-3dB Gain, 0.25 V_{PP} Single Ended Input	12	13		GHz
11.2	SFDR 60 MHz	SFDR14	0.25 Vpp Single Ended Input	50	61		dB
11.3	SFDR 1060 MHz	SFDR15	0.25 Vpp Single Ended Input	52	58		dB
11.4	SFDR 2060 MHz	SFDR16	0.25 Vpp Single Ended Input	42	45		dB
11.5	SFDR 3060 MHz	SFDR17	0.25 Vpp Single Ended Input	35	37		dB
11.6	SFDR 4060 MHz	SFDR18	0.25 Vpp Single Ended Input	34	36		dB
11.7	SFDR 5060 MHz	SFDR19	0.25 Vpp Single Ended Input	30	32		dB
11.8	SFDR 6060 MHz	SFDR20	0.25 Vpp Single Ended Input	28	30		dB
11.9	SFDR 7060 MHz	SFDR21	0.25 Vpp Single Ended Input	26	29		dB
11.10	SFDR 8060 MHz	SFDR22	0.25 Vpp Single Ended Input	25	27		dB
11.11	SFDR 9060 MHz	SFDR23	0.25 Vpp Single Ended Input	23	25		dB
11.12	SFDR 10060 MHz	SFDR24	0.25 Vpp Single Ended Input	24	26		dB
11.13	SFDR 11060 MHz	SFDR25	0.25 Vpp Single Ended Input	24	26		dB
11.14	SFDR 12060 MHz	SFDR26	0.25 Vpp Single Ended Input	23	26		dB
11.15	THD 60 MHz	THD14	0.25 Vpp Single Ended Input		-60	-49	dB
11.16	THD 1060 MHz	THD15	0.25 Vpp Single Ended Input		-58	-52	dB
11.17	THD 2060 MHz	THD16	0.25 Vpp Single Ended Input		-45	-42	dB
11.18	THD 3060 MHz	THD17	0.25 Vpp Single Ended Input		-37	-35	dB
11.19	THD 4060 MHz	THD18	0.25 Vpp Single Ended Input		-36	-34	dB
11.20	THD 5060 MHz	THD19	0.25 Vpp Single Ended Input		-32	-30	dB
11.21	THD 6060 MHz	THD20	0.25 Vpp Single Ended Input		-30	-28	dB
11.22	THD 7060 MHz	THD21	0.25 Vpp Single Ended Input		-28	-26	dB
11.23	THD 8060 MHz	THD22	0.25 Vpp Single Ended Input		-27	-25	dB
11.24	THD 9060 MHz	THD23	0.25 Vpp Single Ended Input		-24	-23	dB
11.25	THD 10060 MHz	THD24	0.25 Vpp Single Ended Input		-25	-24	dB
11.26	THD 11060 MHz	THD25	0.25 Vpp Single Ended Input		-26	-24	dB
11.27	THD 12060 MHz	THD26	0.25 Vpp Single Ended Input		-26	-23	dB
12.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.5Vpp SINGLE ENDED**						
12.1	Bandwidth	BW_H	-3dB Gain, 0.5 V_{PP} Single Ended Input	7	8		GHz
12.2	SFDR 60 MHz	SFDR27	0.5 Vpp Single Ended Input	52	56		dB
12.3	SFDR 1060 MHz	SFDR28	0.5 Vpp Single Ended Input	49	53		dB
12.4	SFDR 2060 MHz	SFDR29	0.5 Vpp Single Ended Input	37	41		dB
12.5	SFDR 3060 MHz	SFDR30	0.5 Vpp Single Ended Input	31	33		dB
12.6	SFDR 4060 MHz	SFDR31	0.5 Vpp Single Ended Input	31	32		dB
12.7	SFDR 5060 MHz	SFDR32	0.5 Vpp Single Ended Input	28	31		dB
12.8	SFDR 6060 MHz	SFDR33	0.5 Vpp Single Ended Input	25	31		dB
12.9	SFDR 7060 MHz	SFDR34	0.5 Vpp Single Ended Input	23	28		dB
12.10	SFDR 8060 MHz	SFDR35	0.5 Vpp Single Ended Input	23	28		dB
12.11	SFDR 9060 MHz	SFDR36	0.5 Vpp Single Ended Input	23	27		dB
12.12	SFDR 10060 MHz	SFDR37	0.5 Vpp Single Ended Input	25	27		dB
12.13	THD 60 MHz	THD27	0.5 Vpp Single Ended Input		-56	-52	dB
12.14	THD 1060 MHz	THD28	0.5 Vpp Single Ended Input		-53	-49	dB
12.15	THD 2060 MHz	THD29	0.5 Vpp Single Ended Input		-41	-37	dB
12.16	THD 3060 MHz	THD30	0.5 Vpp Single Ended Input		-33	-31	dB
12.17	THD 4060 MHz	THD31	0.5 Vpp Single Ended Input		-32	-30	dB
12.18	THD 5060 MHz	THD32	0.5 Vpp Single Ended Input		-29	-26	dB
12.19	THD 6060 MHz	THD33	0.5 Vpp Single Ended Input		-28	-24	dB
12.20	THD 7060 MHz	THD34	0.5 Vpp Single Ended Input		-26	-22	dB
12.21	THD 8060 MHz	THD35	0.5 Vpp Single Ended Input		-26	-22	dB
12.22	THD 9060 MHz	THD36	0.5 Vpp Single Ended Input		-25	-23	dB
12.23	THD 10060 MHz	THD37	0.5 Vpp Single Ended Input		-26	-24	dB

Test Conditions (see notes for specific conditions): Room Temperature; VCC = 5V; VEE = -5.2V; Clocks: 1GHz, 0.6Vpp Differential; Input: 250mV Single-Ended; Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
13.0	**TRACK TO HOLD SWITCHING AND HOLD STATE, TH1**						
13.1	Aperture Delay	ta	After V(CLK1P) - V(CLK1N) Goes Neg.		+50		ps
13.2	Aperture Jitter	Δt	Jitter Free 1-GHz 0.5-Vpp CLK1[1,2]		30		fs
13.3	Settling Time to 1 mV	ts	At Hold Capacitors. ttrack1,min Observed		250		ps
13.4	Differential Pedestal/V_{IN}[3]				-3		%
13.5	Diff. Droop Rate/V_{IN}				-1		%/ns
13.6	Hold Noise[4]		Per Sqrt (Hold Time)			50	μV/√ns
13.7	Maximum Hold Time[5]	$t_{HD1,MAX}$		5	8		ns
14.0	**HOLD TO TRACK SWITCHING AND TRACK STATE, TH1**						
14.1	Acquisition Time to 1 mV[6]	tacq	At Hold Caps, FSR Step At Input		+50		ps
14.2	Max. Acq. Slew Rate	Dvdt,max	At Hold Caps, FSR Step At Input		100	130	fs
14.3	Rise Time	tr1	20 – 80%, 0.5Vpp input, defined at the sampling bridge.			25	ps
		tr2	20 – 80%, 1.0Vpp input, defined at the sampling bridge.		30		ps
14.4	Minimum Track Time	$t_{TR1,MIN}$				0.4	ns
14.5	Recovery Time		Required Accumulated Track Time After $t_{HD1,MAX}$ Violation			4	ns
15.0	**TRACK TO HOLD SWITCHING AND HOLD STATE, TH2**						
15.1	Aperture Delay	ta2	After V(CLK2P) - V(CLK2N) Goes Neg.		+60		ps
15.2	Settling Time to 1 mV[7]	ts2	At DTH Output. ttrack2,min Observed		1000		ps
15.3	Differential Pedestal/V_{IN}[8]				±2.5		%
15.4	Diff. Droop Rate/V_{IN}				-0.05		%/ns
15.5	Hold Noise		Per Sqrt (Hold Time)		25		μV/√ns
15.6	Maximum Hold Time	$t_{HD2,MAX}$		50			ns
16.0	**HOLD TO TRACK SWITCHING AND TRACK STATE, TH2**						
16.1	Minimum Track Time	$t_{TR2,MIN}$	After TH1 in Hold Mode			0.4	ns
16.2	Recovery Time		Required Accumulated Track Time After thold2,max Violation			4	ns

[1] The clock source jitter and the aperture jitter combine in an rms manner to yield the total sampling jitter. See Definition of Terms.
[2] Device aperture jitter increases as the V(CLK1P) – V(CLK1N) slew rate at the zero crossing decreases. See Theory of Operation.
[3] The differential pedestal error is proportional to the input signal. This gain loss may be observed at the DTH output if TH2 is in track mode during the TH1 track to hold transition.
[4] The variance of the hold noise is proportional to the hold time, thold. TH1 and TH2 hold noise, up to the output sampling instant, should be RMS added to the hold mode integrated noise of the DTH.
[5] Maximum hold time is determined by droop of single-ended hold capacitor voltages. The resulting shift of internal operating voltages is not directly observable at the DTH outputs but eventually causes device performance degradation.
[6] TH1 tacq, dvdt,max, and tr also apply to the reconstructed DTH output if sub-sampling a fast-edge repetitive wave form.
[7] Output is settled ta2 + ts2 after CLK2(P/N) downward transition.
[8] The differential pedestal error is proportional to the input signal.

Operating Conditions

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
18.0	**CLOCK INPUTS (CLK1P, CLK1N, CLK2P, CLK2N)**						
18.1	Amplitude[9]	V_{CPP}		200	600	1000	mVpp
18.2	Common Mode Voltage	V_{CCM}		-250	0	250	mV
18.3	CLK1 Frequency	F_{CLK1}		100		1000	MHz
18.4	CLK2 Frequency	F_{CLK2}		10		1000	MHz
19.0	**ANALOG INPUT (INP, INN)**						
19.1	Full Scale Range	FSR				1500	mVpp
19.2	Common Mode Voltage	V_{CM}		-100	0	100	mV
20.0	**DIGITAL INPUT (TMS)[10]**						
20.1	Input High Voltage	V_{IH}		-0.5	0	1	V
20.2	Input Low Voltage	V_{IL}	Open TMS ≈ –1.4V	-1.5	Open	-1.2	V
21.0	**ANALOG OUTPUT (OUTP, OUTN)**						
21.1	Ext. Termination Voltage	V_{TERM}		0	0	0.5	V
21.2	Ext. Termination Resistor	R_{TERM}	Required From Outputs To Vterm		50		Ω
22.0	**POWER SUPPLY REQUIREMENTS**						
22.1	Positive Supply Voltage	VCC		4.75	5.0	5.25	V
22.2	Negative Supply Voltage	VEE		-5.45	-5.2	-4.95	V
23.0	**OPERATING TEMPERATURE[11]**						
23.1	Case Temperature	Tc	Measured at Bottom Plate	-15		85	°C
23.2	Junction Temperature	Tj				125	°C

[9] For > 500 MHz sinusoidal CLK1(P/N), 500 to 700 mVpp amplitude is recommended for combined aperture jitter and clock feed-through performance. At lower clock frequencies, use high amplitude for minimum jitter. See Theory of Operation.

[10] Not available in the BGA package.

[11] The part is designed to function within a junction temperature range of -40 ~ 125°C. For the best performance, operation within the specified temperature range with a proper heatsink attached to the device is recommended. The heatsink should be attached to the bottom of the PCB, on a metal pad connect by thermal vias to the metal pad where the part is soldered.

Pin Description and Pin Out (49 Ball BGA Package)

P/I/O	PIN	NUM.	NAME	FUNCTION
P	A1, A7, B1, B2, B4, B6, B7, C2, C3, C4, C5, C6, D1, D2, D3, D4, D5, D6, D7, E2, E3, E4, E5, E6, F1, F2, F3, F4, F5, F6, F7, G4	32	GND	Power Supply Ground
P	G1, G7	2	VCC	Positive Power Supply
P	A2, A3, A4, A5, A6, B3, B5	7	VEE	Negative Power Supply
I	G2	1	CLK1P	Clock 1 Input: High = TH1 in Track Mode
I	G3	1	CLK1N	Low = TH1 in Hold Mode
I	G5	1	CLK2P	Clock 2 Input: High = TH2 in Track Mode
I	G6	1	CLK2N	Low = TH2 in Hold Mode
I	C1	1	INN	Analog Input
I	E1	1	INP	
O	C7	1	OUTP	Analog Output
O	E7	1	OUTN	

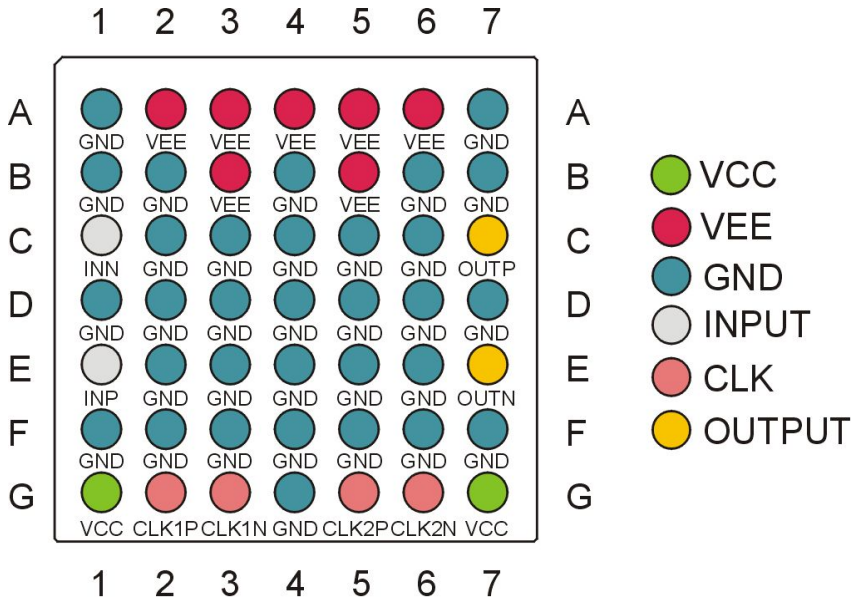

Figure 2 - RTH050 pinout (top view) 49 Ball BGA package.

Pin Description and Pin Out (13 Lead HSD Package)

P/I/O	PIN	NUM.	NAME	FUNCTION
P	Bottom Plate	-	GND	Power Supply Ground
P	11, 13	2	VCC	Positive Power Supply, +5.0V
P	10,12		VEE	Negative Power Supply, -5.2V
I	4	1	CLK1P	Clock 1 Input: High = TH1 in Track Mode Low = TH1 in Hold Mode
I	5	1	CLK1N	Complementary Clock 1 Input
I	6	1	CLK2P	Clock 2 Input: High = TH2 in Track Mode Low = TH2 in Hold Mode
I	7	1	CLK2N	Complementary Clock 2 Input
I	2	1	INP	Analog Input
I	1	1	INN	Complementary Analog Input
I	3	1	TMS	Track Mode Select: Open = Sampled operation Ground = TH1 and TH2 in Track Mode
O	9	1	OUTP	Analog Output
O	8	1	OUTN	Complementary Analog Output

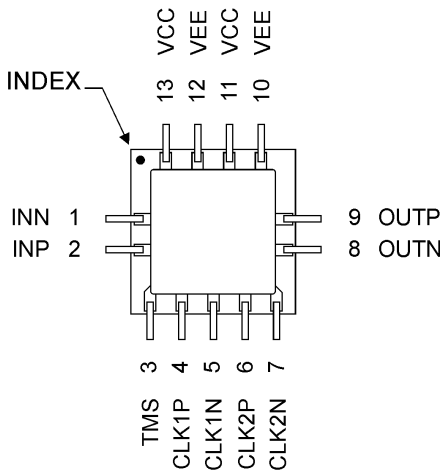

Figure 3 - RTH050 pinout (top view) 13 lead HSD Package.

Pin Description and Pin Out (24 Lead QFP Package)

P/I/O	PIN	NUM.	NAME	FUNCTION
P	Bottom Plate	-	GND	Power Supply Ground
P	2, 4, 6, 10, 14, 16, 18, 20, 22, 24	10	GND	Power Supply Ground
P	1, 21	2	VCC	Positive Power Supply, +5.0V
P	19, 23	2	VEE	Negative Power Supply, -5.2V
I	8	1	CLK1P	Clock 1 Input: High = TH1 in Track Mode Low = TH1 in Hold Mode
I	9	1	CLK1N	Complementary Clock 1 Input
I	11	1	CLK2P	Clock 2 Input: High = TH2 in Track Mode Low = TH2 in Hold Mode
I	12	1	CLK2N	Complementary Clock 2 Input
I	5	1	INP	Analog Input
I	3	1	INN	Complementary Analog Input
I	7	1	TMS	Track Mode Select: Open = Sampled operation Ground = TH1 and TH2 in Track Mode
O	17	1	OUTP	Analog Output
O	15	1	OUTN	Complementary Analog Output
R	13	1	NC	Reserved

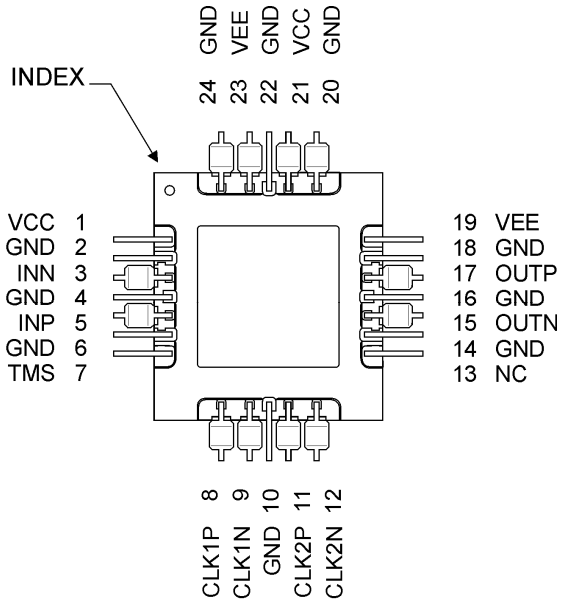

Figure 4 - RTH050 pinout (top view) 24 lead QFP package.

Definitions of Terms

Acquisition Time (tacq). The delay between the time a track-and-hold circuit (TH) enters track mode and the time the TH hold capacitor nodes track the input within some specified precision. The acquisition time sets a lower limit on the required track time during clocked operation.

Aperture Delay (ta). The average (or mean value) of the delay between the hold command (input clock switched from hold to track state) and the instant at which the analog input is sampled. The time is positive if the clock path delay is longer than the signal path delay. It is negative if the signal path delay is longer than the clock path delay.

Aperture Jitter (Δt). The standard deviation of the delay between the hold command (input clock switched from track-to-hold state) and the instant at which the analog input is sampled, excluding clock source jitter. It is the total jitter if the clock source is jitter free (ideal). Jitter diverges slowly as measurement time increases because of "1/f" noise, important at low frequencies (< 10 kHz). The specified jitter takes into account the white noise sources only (thermal and shot noise). For high-speed samplers this is reasonable, since even long data records span a time shorter than the time scale important for 1/f noise. For white-noise caused jitter, the clock and aperture jitter can be added in an rms manner to obtain the total sampling jitter.

If the underlying voltage noise mechanism of the sampling jitter has a white spectrum, the sampled signal will display a white noise floor as well. In this case, the required aperture jitter, Δt, to achieve a certain SNR, for a full-scale sinewave at frequency, *f*, is given by (B. Razavi, Principles of Data Conversion, IEEE Press, 1995, Appendix 2.1):

$$SNR\,(dB) = -20\log(2\pi f \Delta t)$$

If this TH is used in front of an *n*-bit ADC, then the ideal ADC SNDR is given by:

$$SNDR\,(dB) = 10\log(3/2) + 20\log(2)n = 1.76 + 6.02n$$

In order that the TH jitter performance do not limit the ADC performance, the jitter must fulfill:

$$\Delta t \le \frac{1}{\sqrt{6}\pi 2^n f}\,.$$

Note that this is independent of the sampling rate, so undersampling does not improve jitter tolerance. The averaging that is often combined with undersampling in test equipment, does improve jitter tolerance (and tolerance to other white noise effects).

The criterion above is sharper than the standard (incorrect) time-domain slope estimate by a factor √6. The reason is that *n*-bit quantization requires an rms error of (quantization step)/√12, which is considerably smaller than the quantization step error implicitly allowed in the usual time-domain estimates (another √2 comes from the energy of a sine wave relative to its amplitude squared).

The time-domain maximum slope argument can be appropriate for non-sinusoidal inputs, such as those encountered in instrumentation. If the rms error, ΔV, in the maximum slope region, slope FSR/(rise time), is used to define an effective number of bits, *n*, then the jitter simply needs to fulfill:

$$\Delta t \le \frac{rise\ time}{2^n}$$

Clock Jitter. The standard deviation of the mid-points of the relevant (rising or falling) edge of the clock source relative to the ideal edge (best fit). This jitter can be derived from the phase noise of the clock source, where the lower frequency bound of integration should correspond to the duration of a measurement record that the source will be used for.

Common-Mode Rejection Ratio (CMRR). Proportionality coefficient of the differential output and the common mode component of input signal. If an ideal symmetric input is available, CMR is the ratio of the differential output to the input on either input pin. A high-quality 50-ohm splitter may be used to generate the symmetrical inputs.

Full Scale Range (FSR). The maximum difference between the highest and lowest input levels for which various device performance specifications hold, unless otherwise noted.

Gain. Ratio of output signal magnitude to input signal magnitude. For sinewave inputs, it is the ratio of the amplitude of the first (main) harmonic output (HD1) to the amplitude of the input.

Input Bandwidth (BW, bw). The input frequency at which the gain for sinewave input is reduced by 3

dB (factor 1/√2) relative to its average value at low frequencies. The low frequency range is defined as the range including DC over which the gain stays essentially constant. The high frequency range is characterized by an increase in gain variation versus frequency, at least including the eventual monotonic decrease of the gain ("roll-off"). The input bandwidth tends to be input amplitude dependent. It is normally largest for very small inputs (small signal bandwidth, bw) and smallest for FSR inputs (large signal bandwidth, BW).

Settling Time (ts). The delay between the time that a track-and-hold circuit (TH) enters hold mode and the time that the TH hold capacitor nodes settle to within some specified precision. The settling time sets a lower limit on the required hold time during clocked operation.

Spectrum. The finite Fourier transform (FFT) of the discrete-time-sampled TH output. Ideally, this is obtained with a very high-resolution ADC quantizing the TH output with a clock rate locked to the TH clock (the ADC may be clocked at a slower rate than the TH). In the case of a dual TH (DTH), we can also use the beat frequency test, where the input frequency is close to an integer multiple of the clock frequency, and the DTH output is fed directly into a spectrum analyzer. The DTH output then contains little high frequency energy and the low frequency part of the spectrum analyzer sweep accurately represents the TH spectrum that would have been obtained with the ADC method.

Spurious Free Dynamic Range (SFDR). The ratio of the magnitude of the first (main) harmonic, HD1, and the highest other harmonic (or nonharmonic other tone, if present), as observed in the TH spectrum. The input is FSR, unless otherwise noted. SFDR in dB is given by 20log (SFDR as amplitude ratio), and is generally positive.

Total Harmonic Distortion (THD). The ratio of the square root of the sum of the harmonics 2 to 5 to the amplitude of the first (main) harmonic in the TH spectrum. THD in dB is given by 20log (THD as amplitude ratio), and is generally negative.

Theory of Operation

The DTH chip contains two TH's, TH1 and TH2, in series, together with clock shaping circuitry, BUFFER1 and BUFFER2, and a 50-ohm output driver, OUTBUF (Figure 1). To maximize dynamic range and insensitivity to noise, all non-DC internal circuits and all non-DC inputs and outputs are differential. TH1 determines the dynamic sampled-mode performance of the DTH. Its sampling bridges exploit the ultra-high speed of the Schottky diodes available in the GaAs HBT process. TH1 clock inputs, CLK1P and CLK1N, should be driven by a low-jitter clock source. TH2 is similar to TH1, except that its bandwidth requirement is lower and its gain is closer to unity.

The DTH receives a differential analog input signal at inputs INP and INN, which is sampled on the TH1 hold capacitors upon a falling transition of its differential clock voltage V(CLK1P) – V(CLK1N), after an aperture delay, ta, see Figure 3. TH1's aperture delay is positive, nominally 60ps.

The sampling instant is affected by clock source jitter (off-chip) and aperture jitter (caused by on-chip noise). From the Definition of Terms, the required total sampling jitter for sampling a 1 GHz 1 Vpp sine wave with 10-bit accuracy is 127 fs. The aperture jitter of the RTH050 is less than 100 fs for a 1 GHz 0.5 Vpp TH1 clock, CLK1. Using rms addition of jitter, the clock source jitter must be less than 80 fs (over the measurement record time) for direct 10-bit sampling of GHz range signals. Given a noise variance, ΔV, of the on-chip clock buffer, its aperture jitter, Δt, is inversely proportional to the clock buffer gain and the slew rate of the incoming clock at the zero-crossing point:

$$\Delta t = \frac{\Delta V}{gain \times slew\ rate}\ .$$

For low slew rates or frequencies, the clock buffer gain is constant and its aperture jitter is inversely proportional to the input clock slew rate, improving with increasing slew rate. For high slew rates or high frequencies, the jitter increases again, because the buffer gain drops steeply. For the RTH050, the clock buffer gain is still roughly constant up to 1 GHz, so that the aperture jitter is inversely proportional with

the slew rate of the incoming clock. In the above equation, we have $\Delta V/gain \approx 0.15$ mV. The RTH050 aperture jitter at various slew rates can then be estimated. For example, a 1 GHz 0.5 Vpp sinusoidal CLK1 signal corresponds to a slew rate ~ 1.6 V/ns, correctly yielding an aperture jitter < 100 fs.

The held and buffered output of TH1, VTH1, is sampled on the TH2 hold capacitors upon a falling transition of its differential clock voltage V(CLK2P) – V(CLK2N), after an aperture delay closely equal to that of TH1. This allows simple out-of-phase clocking of TH1 and TH2 by having opposite phases for CLK1 and CLK2. Aperture jitter of TH2 is irrelevant, since the slew rate of the TH2 input is equal to the TH1 differential droop rate, about 1000x lower than the input slew rate for TH1 for a 1 GHz 1 Vpp sine wave. TH2 can be in track mode before TH1 switches to hold, but a minimum track time of TH2 after TH1 enters hold mode must be observed to ensure that TH2 has fully acquired the TH1 output (ttrack2, min).

Hold mode feedthrough, or in to out hold-mode gain in dB, again is important for TH1 and not for TH2, since any distortion on the held TH1 signal by a rapidly varying TH1 input will be sampled by TH2, and can not be removed. RTH050's TH1 hold mode feedthrough performance is more than sufficient for 10 bit sampling of GHz range signals.

After a TH1 postamplifier, TH2 produces an output VTH2. For out-of-phase clocking, the delay from the hold instant of TH1 to the ideal sampling time of circuitry after TH2 is close to one full clock cycle, for example 1 ns at a 1 GHz sampling rate. The TH2 output is flat for more than half a clock cycle, which eases the bandwidth requirement of subsequent circuitry. This is true, even though a small glitch will be present at the transition from track to hold of TH2 and the output is only 10 bit accurate during the latter part of half a clock cycle.

Lower limits for the sampling rates of TH1 and TH2 are set by single-ended hold-mode droop rates, and lead to the specification of maximum hold times (thold1, max and thold2, max). For longer hold times, the DTH must be allowed sufficient recovery time during track phase (or a sequence of track phases), so it can return to normal operation mode. The bandwidth of subsequent circuitry can be minimal if TH2 is clocked at its lowest recommended frequency, 10 MHz. Since TH1 should be clocked at least at 100 MHz, and possibly faster to meet jitter requirements, CLK1 and CLK2 can be chosen different, as long as they are locked to each other with a proper phase relationship. Minimum required single-pole bandwidth at the output for 10-bit precision is $(10\ln 2/2\pi) \times f_{CLK2}$, or approximately $1.1 f_{CLK2}$. In practice, <20 MHz bandwidth of subsequent circuitry would be sufficient, if f_{CLK2} is 10 MHz.

One digital input, Track Mode Select (TMS), is provided to put both TH's in track mode, independent of the clock signals. The bandwidth of the DTH is substantially lower in this mode than in the sampled mode. The TMS is useful for low sample-rate operation, including DC testing.

Signal Descriptions

The RTH050 inputs are terminated on-chip with 50 Ω to GND. This automatically protects against off-chip high-impedance high-voltage disturbances. The absolute maximum rated voltage at input termination resistors is ±1 V, at 20 mA current. The RTH050 is designed for 1 Vpp differential input signals, and can accept common-mode offsets up to ±100 mV. If operated in single-ended mode, terminate the complementary input off-chip with 50 Ω to the same common mode as the driven input. The single-ended FSR is half that of the differential FSR. Distortion in the single-ended mode can be up to 6 dB higher than in differential mode, and differential input should be used for optimal performance. The INP and INN inputs are equivalent, except for the polarity of their effect on OUTP and OUTN.

All four clock input signals are terminated on-chip with 50 Ω to GND. Use differential clock signals for optimal performance. Large CLK1 edge rate benefits aperture jitter performance, small CLK1 and CLK2 amplitudes minimizes distortion due to clock feed-through in the higher clock frequency range (500 to 1000 MHz). In case of single-ended clocking the complementary input(s) can be terminated directly to GND (lowest noise, clock waveform distortion is not critical). Distortion for single-ended clocks can be several dB higher than for differential clocks, and differential clocks should be used for optimal performance.

The track-mode select, TMS, can simply be left open for the (default) sampled-mode operation of the RTH050. Grounding the TMS puts both track-and-holds, TH1 and TH2, in track-mode. In this state, the TMS draws up to 0.75 mA of current.

Due to its highly differential design, the RTH050 requires relatively modest power supply decoupling. The 0.01 μF capacitors VEE to GND and VEE to VCC (Figure 4) should be placed as close to the package as possible. Larger low frequency power supply decoupling capacitors, VEE to GND and VCC to GND, should be placed within 1 inch of the RTH050. Depending on the expected noise on the supplies more capacitors in parallel may need to be used. With low-impedance supplies that are very quiet (no digital circuitry), the RTH050 can also perform well with no external decoupling at all.

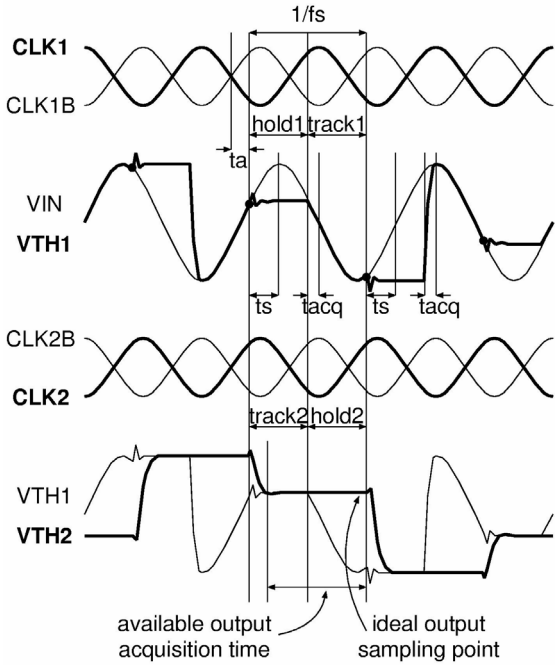

Figure 5 - Timing diagram for out-of-phase clocking of TH1 and TH2

Typical Operating Circuit

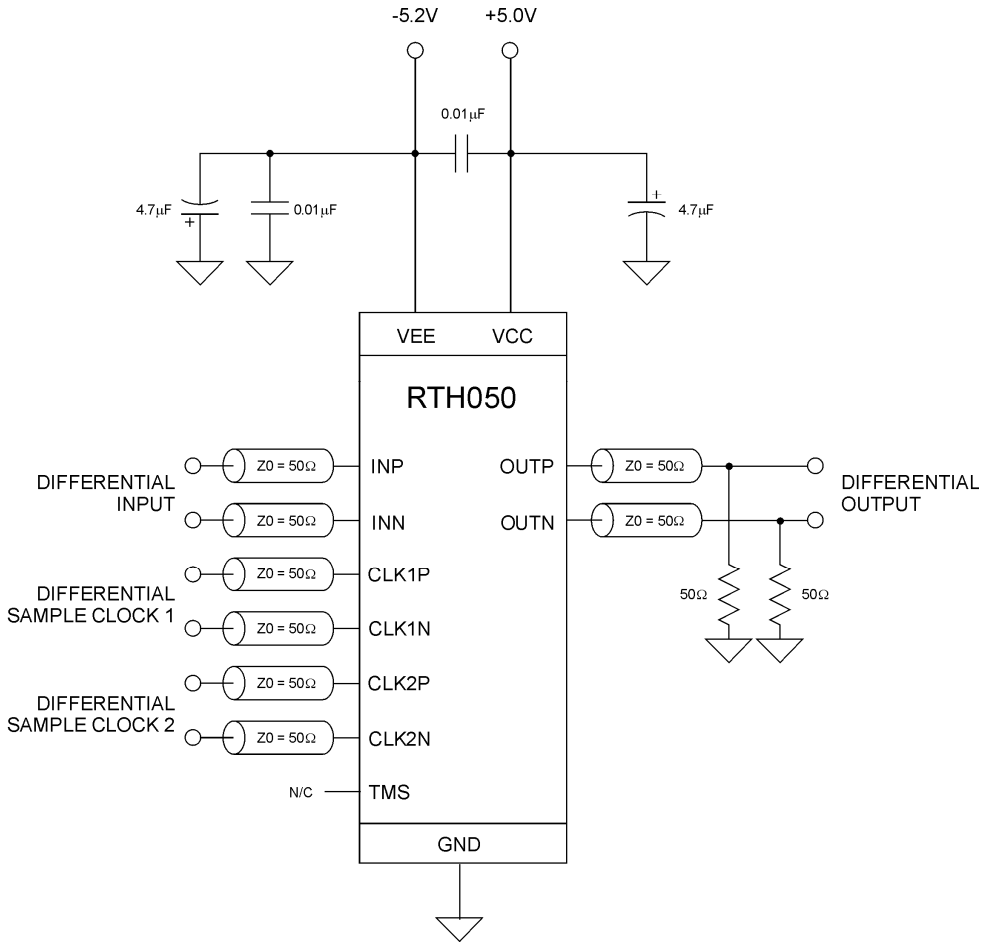

Figure 6 - Typical interface circuit (sampled mode, connect TMS to GND for track mode)
All differential inputs are terminated on-chip with 50 Ω to GND.

Typical Performance

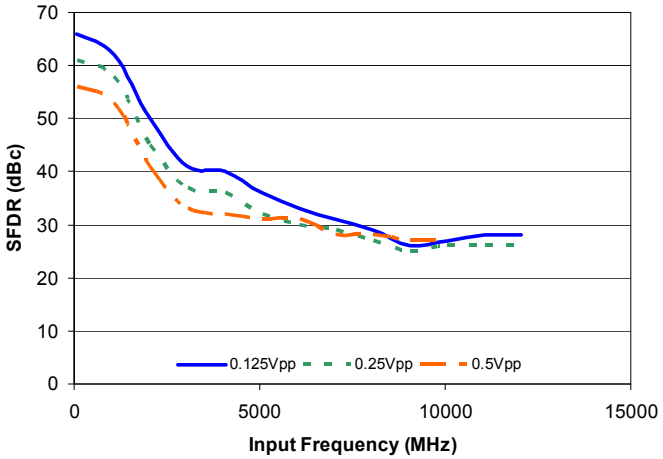

Figure 7. SFDR x Fin, single tone.

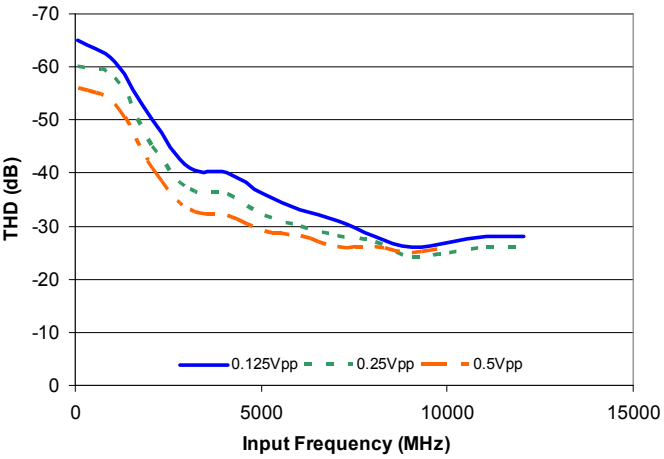

Figure 8. THD x Fin, single tone.

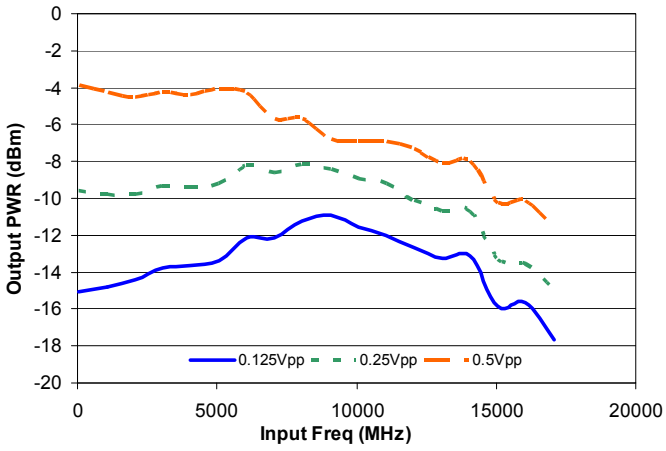

Figure 9. Input bandwidth.

Die Plot and Pad Arrangement

The inputs and output of the RTH050 are arranged in a ground-signal-ground-signal-ground (GSGSG) configuration on opposite sides of the die. The clock signals come in under an orthogonal direction, which reduces inductive coupling to the signal path, both for bond wires and for package leads. The part does not require other components inside the package, since sufficient bypass capacitance is supplied on-chip.

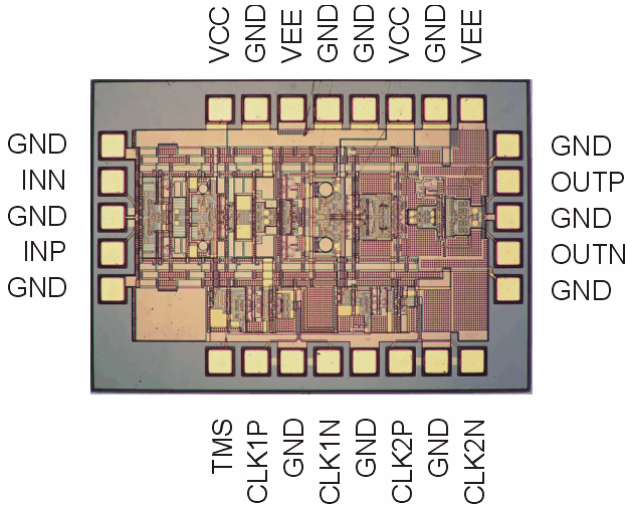

Figure 10 - RTH050 die photo and pad arrangement; Die size: 75 x 55 x 7 mils (1.899 x 1.375 x 0.178 mm); Pad pitch: 5.91 mil (0.150 mm); Die photograph for pad placement reference only.

Package Information -BG

The package is a high-speed 49 Ball BGA.

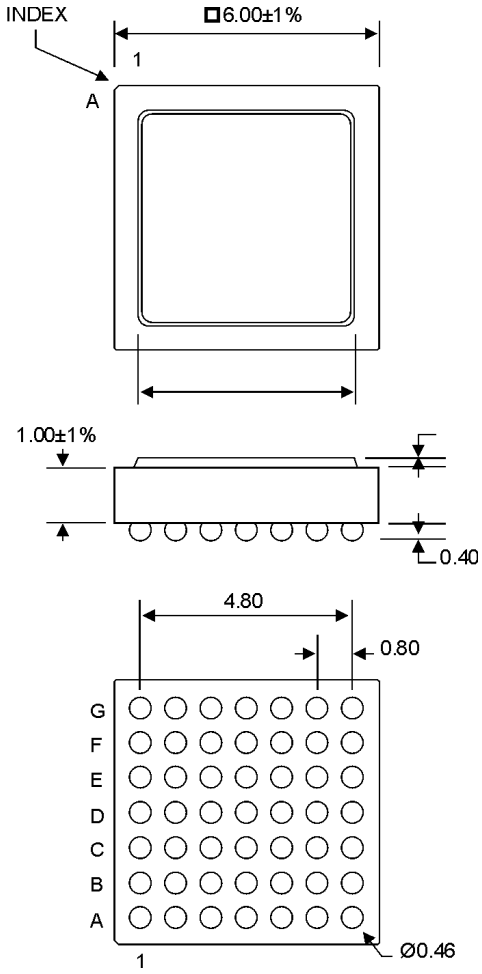

Figure 11 - RTH050-BG package outline, dimensions in mm.

Package Information -HD

The package is a 13 lead HSD with the leads trimmed to 0.040 inch (1.02 mm) in length. The thermal impedance (junction to base) is approximately 8 °C/W.

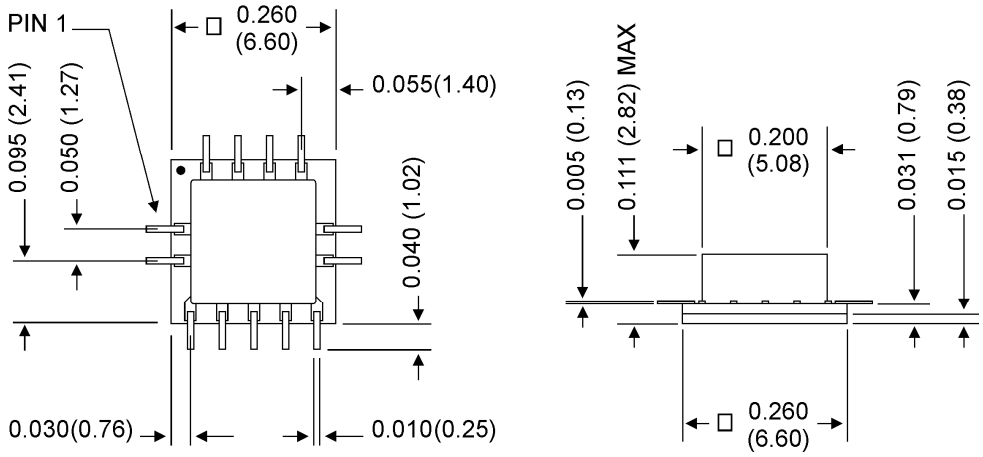

Figure 12 - RTH050-HD package outline, dimensions in inches (mm), tolerance ±0.003" (±0.072mm).

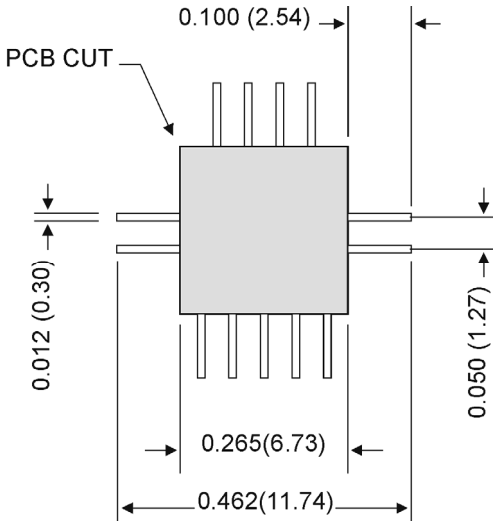

Figure 13 - RTH050-HD footprint, dimensions shown in inches (mm).

Package Information -HQ

The package is a high-speed 24 lead QFP with a Cu/Mo metal pad at the bottom.

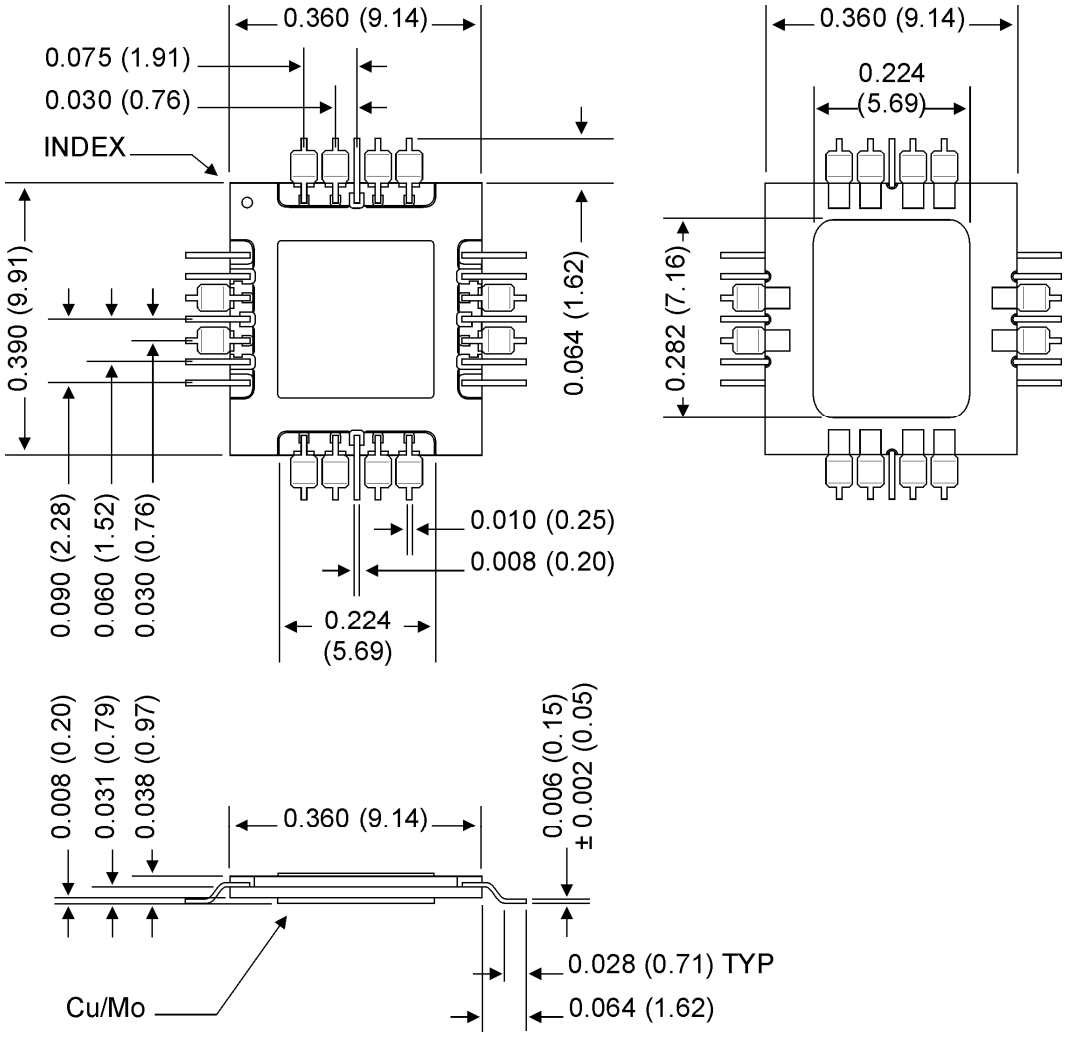

Figure 14 - RTH050-HQ package outline, dimensions in inches (mm).