TELEDYNE
SCIENTIFIC COMPANY

RTH070

20 GHz Bandwidth High Linearity Track-and-Hold

REV-DATE PA1-2412
FILE DS_0132PA1-2412

DS

RTH070

20 GHz Bandwidth High Linearity Track-and-Hold

Features

- 20 GHz Input Bandwidth
- Better than -45dBc THD Over the Total Bandwidth with Small Signal Input
- Better than 45dBc SFDR Over the Total Bandwidth with Small Signal Input
- 1000 - 4000 MHz Sampling Rate
- Differential Analog Input/Output
- Output Held more than Half Clock Cycle
- 1.5W Power Dissipation
- Single Power Supply

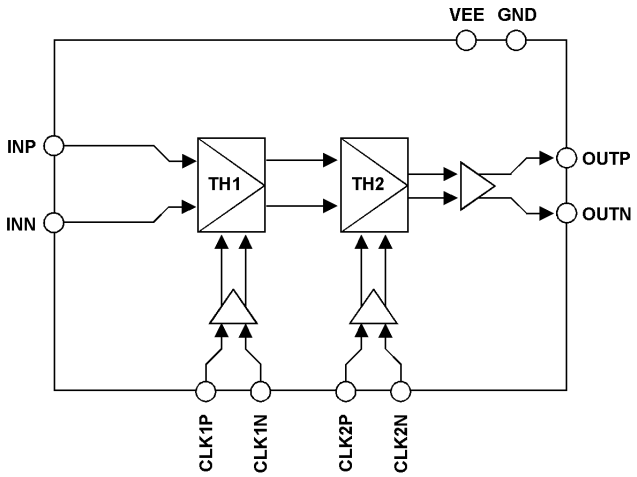

Figure 1 - Functional Block Diagram

Product Description

RTH070's bandwidth and aperture jitter enable 1 GS/s accurate sampling of DC to multi-GHz signals. The differential-to-differential dual track-and-hold cascades two track-and-hold circuits, TH1 and TH2. The RTH070 provides a held output for more than half a clock cycle, easing bandwidth requirements of subsequent circuitry relative to the case of a single track-and-hold (TH). The option to independently clock TH1 and TH2 further relaxes this requirement for sub-sampling applications.

Ordering information

PART NUMBER	DESCRIPTION
RTH070-HQ	24 Pin QFP Package
RTH070-DI	Die
EVRTH070	Evaluation Module

CAUTION
DEVICE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)

Absolute Maximum Ratings

Supply Voltages

VEE to GND ……..…….…..... -6 V

Input Voltages

INP, INN to GND ……..……..…….-1 V
CLK1P, CLK1N, CLK2P, CLK2N to GND …….…..... -1 V

Temperature

Case Temperature ……..…….....+125 °C
Junction Temperature ……..…….. +150 °C
Lead, Soldering (10 Seconds) ……..…….. +220 °C
Storage …….…….. -40 to 125 °C

DC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.4V; Clock: 1GHz, 0.4Vpp Differential; Input: 300mV Single-Ended; Differential Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
1.0	**DC TRANSFER FUNCTION**						
1.1	Gain	G			-1.7		dB
2.0	**TEMPERATURE DRIFT**						
2.1	Warm-up Time		After Power-up		0		s
3.0	**ANALOG INPUT (INP, INN)**						
3.1	Common Mode Voltage	IN_{CM}	Self Bias		-650		mV
3.2	Input Impedance	R_{IIN}			50		Ω
4.0	**CLOCK INPUTS (CLK1P, CLK1N, CLK2P, CLK2N)**						
4.1	Input Resistance	R_{CIN}	Each Lead to GND		50		Ω
5.0	**ANALOG OUTPUT (OUTP, OUTN)**						
5.1	Output Resistance	R_{OUT}	Each Output to GND		50		Ω
5.2	Maximum Current		Into Output Lead			16	mA
5.3	Output Offset Voltage	V_{OFF}	Absolute Value (No Input Signal)		20		mV
6.0	**POWER SUPPLY REQUIREMENTS**						
6.1	Negative Supply Current	IEE			280		mA
6.2	Power Dissipation	P			1.5		W

AC Electrical Specification – CLK = 1GHz

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.4V; Clock: 1GHz, 0.4Vpp Differential; Differential Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
7.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.1Vpp SINGLE ENDED**						
7.1	Bandwidth	BW	-3dB Gain, 0.1 V_{PP} Single Ended Input		20		GHz
7.2	SFDR						
	60 MHz	SFDR	0.1 Vpp Single Ended Input		62		dBc
	2060 MHz	SFDR	0.1 Vpp Single Ended Input		61		dBc
	4060 MHz	SFDR	0.1 Vpp Single Ended Input		61		dBc
	6060 MHz	SFDR	0.1 Vpp Single Ended Input		56		dBc
	8060 MHz	SFDR	0.1 Vpp Single Ended Input		55		dBc
	10060 MHz	SFDR	0.1 Vpp Single Ended Input		54		dBc
	12060 MHz	SFDR	0.1 Vpp Single Ended Input		48		dBc
	14060 MHz	SFDR	0.1 Vpp Single Ended Input		48		dBc
	16060 MHz	SFDR	0.1 Vpp Single Ended Input		52		dBc
	18060 MHz	SFDR	0.1 Vpp Single Ended Input		52		dBc
	20060 MHz	SFDR	0.1 Vpp Single Ended Input		47		dBc
7.3	THD						
	60 MHz	THD	0.1 Vpp Single Ended Input		-57		dBc
	2060 MHz	THD	0.1 Vpp Single Ended Input		-56		dBc
	4060 MHz	THD	0.1 Vpp Single Ended Input		-55		dBc
	6060 MHz	THD	0.1 Vpp Single Ended Input		-52		dBc
	8060 MHz	THD	0.1 Vpp Single Ended Input		-51		dBc
	10060 MHz	THD	0.1 Vpp Single Ended Input		-51		dBc
	12060 MHz	THD	0.1 Vpp Single Ended Input		-46		dBc
	14060 MHz	THD	0.1 Vpp Single Ended Input		-46		dBc
	16060 MHz	THD	0.1 Vpp Single Ended Input		-48		dBc
	18060 MHz	THD	0.1 Vpp Single Ended Input		-47		dBc
	20060 MHz	THD	0.1 Vpp Single Ended Input		-45		dBc
8.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.2Vpp SINGLE ENDED**						
8.1	Bandwidth	BW	-3dB Gain, 0.2 V_{PP} Single Ended Input		20		GHz
8.2	SFDR						
	60 MHz	SFDR	0.2 Vpp Single Ended Input		67		dBc
	2060 MHz	SFDR	0.2 Vpp Single Ended Input		64		dBc
	4060 MHz	SFDR	0.2 Vpp Single Ended Input		60		dBc
	6060 MHz	SFDR	0.2 Vpp Single Ended Input		51		dBc
	8060 MHz	SFDR	0.2 Vpp Single Ended Input		53		dBc
	10060 MHz	SFDR	0.2 Vpp Single Ended Input		50		dBc
	12060 MHz	SFDR	0.2 Vpp Single Ended Input		42		dBc
	14060 MHz	SFDR	0.2 Vpp Single Ended Input		42		dBc
	16060 MHz	SFDR	0.2 Vpp Single Ended Input		48		dBc
	18060 MHz	SFDR	0.2 Vpp Single Ended Input		48		dBc
	20060 MHz	SFDR	0.2 Vpp Single Ended Input		44		dBc
8.3	THD						
	60 MHz	THD	0.2 Vpp Single Ended Input		-62		dBc
	2060 MHz	THD	0.2 Vpp Single Ended Input		-60		dBc
	4060 MHz	THD	0.2 Vpp Single Ended Input		-57		dBc
	6060 MHz	THD	0.2 Vpp Single Ended Input		-50		dBc
	8060 MHz	THD	0.2 Vpp Single Ended Input		-50		dBc
	10060 MHz	THD	0.2 Vpp Single Ended Input		-48		dBc
	12060 MHz	THD	0.2 Vpp Single Ended Input		-41		dBc
	14060 MHz	THD	0.2 Vpp Single Ended Input		-41		dBc
	16060 MHz	THD	0.2 Vpp Single Ended Input		-45		dBc
	18060 MHz	THD	0.2 Vpp Single Ended Input		-45		dBc
	20060 MHz	THD	0.2 Vpp Single Ended Input		-41		dBc

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.4V; Clock: 1GHz, 0.4Vpp Differential; Differential Outputs Terminated Into 50 Ω to 0V.

9.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.3Vpp SINGLE ENDED**						
9.1	Bandwidth	BW	-3dB Gain, 0.3 V_{PP} Single Ended Input		20		GHz
9.2	SFDR						
	60 MHz	SFDR	0.3 Vpp Single Ended Input		62		dBc
	2060 MHz	SFDR	0.3 Vpp Single Ended Input		61		dBc
	4060 MHz	SFDR	0.3 Vpp Single Ended Input		57		dBc
	6060 MHz	SFDR	0.3 Vpp Single Ended Input		51		dBc
	8060 MHz	SFDR	0.3 Vpp Single Ended Input		56		dBc
	10060 MHz	SFDR	0.3 Vpp Single Ended Input		49		dBc
	12060 MHz	SFDR	0.3 Vpp Single Ended Input		38		dBc
	14060 MHz	SFDR	0.3 Vpp Single Ended Input		38		dBc
	16060 MHz	SFDR	0.3 Vpp Single Ended Input		44		dBc
	18060 MHz	SFDR	0.3 Vpp Single Ended Input		44		dBc
	20060 MHz	SFDR	0.3 Vpp Single Ended Input		40		dBc
9.3	THD						
	60 MHz	THD	0.3 Vpp Single Ended Input		-60		dBc
	2060 MHz	THD	0.3 Vpp Single Ended Input		-58		dBc
	4060 MHz	THD	0.3 Vpp Single Ended Input		-54		dBc
	6060 MHz	THD	0.3 Vpp Single Ended Input		-50		dBc
	8060 MHz	THD	0.3 Vpp Single Ended Input		-52		dBc
	10060 MHz	THD	0.3 Vpp Single Ended Input		-48		dBc
	12060 MHz	THD	0.3 Vpp Single Ended Input		-38		dBc
	14060 MHz	THD	0.3 Vpp Single Ended Input		-38		dBc
	16060 MHz	THD	0.3 Vpp Single Ended Input		-42		dBc
	18060 MHz	THD	0.3 Vpp Single Ended Input		-42		dBc
	20060 MHz	THD	0.3 Vpp Single Ended Input		-38		dBc

AC Electrical Specification – CLK = 2GHz

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.4V; Clock: 2GHz, 0.4Vpp Differential; Differential Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
10.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.1Vpp SINGLE ENDED**						
10.1	Bandwidth	BW	-3dB Gain, 0.1 V_{PP} Single Ended Input		20		GHz
10.2	SFDR						
	60 MHz	SFDR	0.1 Vpp Single Ended Input		63		dBc
	2060 MHz	SFDR	0.1 Vpp Single Ended Input		62		dBc
	4060 MHz	SFDR	0.1 Vpp Single Ended Input		63		dBc
	6060 MHz	SFDR	0.1 Vpp Single Ended Input		56		dBc
	8060 MHz	SFDR	0.1 Vpp Single Ended Input		57		dBc
	10060 MHz	SFDR	0.1 Vpp Single Ended Input		54		dBc
	12060 MHz	SFDR	0.1 Vpp Single Ended Input		47		dBc
	14060 MHz	SFDR	0.1 Vpp Single Ended Input		47		dBc
	16060 MHz	SFDR	0.1 Vpp Single Ended Input		55		dBc
	18060 MHz	SFDR	0.1 Vpp Single Ended Input		53		dBc
	20060 MHz	SFDR	0.1 Vpp Single Ended Input		50		dBc
10.3	THD						
	60 MHz	THD	0.1 Vpp Single Ended Input		-58		dBc
	2060 MHz	THD	0.1 Vpp Single Ended Input		-58		dBc
	4060 MHz	THD	0.1 Vpp Single Ended Input		-58		dBc
	6060 MHz	THD	0.1 Vpp Single Ended Input		-53		dBc
	8060 MHz	THD	0.1 Vpp Single Ended Input		-54		dBc
	10060 MHz	THD	0.1 Vpp Single Ended Input		-53		dBc
	12060 MHz	THD	0.1 Vpp Single Ended Input		-47		dBc
	14060 MHz	THD	0.1 Vpp Single Ended Input		-47		dBc
	16060 MHz	THD	0.1 Vpp Single Ended Input		-52		dBc
	18060 MHz	THD	0.1 Vpp Single Ended Input		-51		dBc
	20060 MHz	THD	0.1 Vpp Single Ended Input		-47		dBc
11.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.2Vpp SINGLE ENDED**						
11.1	Bandwidth	BW	-3dB Gain, 0.2 V_{PP} Single Ended Input		20		GHz
11.2	SFDR						
	60 MHz	SFDR	0.2 Vpp Single Ended Input		68		dBc
	2060 MHz	SFDR	0.2 Vpp Single Ended Input		65		dBc
	4060 MHz	SFDR	0.2 Vpp Single Ended Input		62		dBc
	6060 MHz	SFDR	0.2 Vpp Single Ended Input		50		dBc
	8060 MHz	SFDR	0.2 Vpp Single Ended Input		53		dBc
	10060 MHz	SFDR	0.2 Vpp Single Ended Input		49		dBc
	12060 MHz	SFDR	0.2 Vpp Single Ended Input		41		dBc
	14060 MHz	SFDR	0.2 Vpp Single Ended Input		41		dBc
	16060 MHz	SFDR	0.2 Vpp Single Ended Input		49		dBc
	18060 MHz	SFDR	0.2 Vpp Single Ended Input		47		dBc
	20060 MHz	SFDR	0.2 Vpp Single Ended Input		45		dBc
11.3	THD						
	60 MHz	THD	0.2 Vpp Single Ended Input		-63		dBc
	2060 MHz	THD	0.2 Vpp Single Ended Input		-61		dBc
	4060 MHz	THD	0.2 Vpp Single Ended Input		-59		dBc
	6060 MHz	THD	0.2 Vpp Single Ended Input		-50		dBc
	8060 MHz	THD	0.2 Vpp Single Ended Input		-52		dBc
	10060 MHz	THD	0.2 Vpp Single Ended Input		-48		dBc
	12060 MHz	THD	0.2 Vpp Single Ended Input		-41		dBc
	14060 MHz	THD	0.2 Vpp Single Ended Input		-41		dBc
	16060 MHz	THD	0.2 Vpp Single Ended Input		-47		dBc
	18060 MHz	THD	0.2 Vpp Single Ended Input		-46		dBc
	20060 MHz	THD	0.2 Vpp Single Ended Input		-43		dBc

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.4V; Clock: 1GHz, 0.4Vpp Differential; Differential Outputs Terminated Into 50 Ω to 0V.

12.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.3Vpp SINGLE ENDED**						
12.1	Bandwidth	BW	-3dB Gain, 0.3 V_{PP} Single Ended Input		20		GHz
12.2	SFDR						
	60 MHz	SFDR	0.3 Vpp Single Ended Input		62		dBc
	2060 MHz	SFDR	0.3 Vpp Single Ended Input		61		dBc
	4060 MHz	SFDR	0.3 Vpp Single Ended Input		57		dBc
	6060 MHz	SFDR	0.3 Vpp Single Ended Input		50		dBc
	8060 MHz	SFDR	0.3 Vpp Single Ended Input		53		dBc
	10060 MHz	SFDR	0.3 Vpp Single Ended Input		48		dBc
	12060 MHz	SFDR	0.3 Vpp Single Ended Input		38		dBc
	14060 MHz	SFDR	0.3 Vpp Single Ended Input		38		dBc
	16060 MHz	SFDR	0.3 Vpp Single Ended Input		43		dBc
	18060 MHz	SFDR	0.3 Vpp Single Ended Input		44		dBc
	20060 MHz	SFDR	0.3 Vpp Single Ended Input		40		dBc
12.3	THD						
	60 MHz	THD	0.3 Vpp Single Ended Input		-60		dBc
	2060 MHz	THD	0.3 Vpp Single Ended Input		-58		dBc
	4060 MHz	THD	0.3 Vpp Single Ended Input		-55		dBc
	6060 MHz	THD	0.3 Vpp Single Ended Input		-49		dBc
	8060 MHz	THD	0.3 Vpp Single Ended Input		-52		dBc
	10060 MHz	THD	0.3 Vpp Single Ended Input		-47		dBc
	12060 MHz	THD	0.3 Vpp Single Ended Input		-38		dBc
	14060 MHz	THD	0.3 Vpp Single Ended Input		-38		dBc
	16060 MHz	THD	0.3 Vpp Single Ended Input		-42		dBc
	18060 MHz	THD	0.3 Vpp Single Ended Input		-41		dBc
	20060 MHz	THD	0.3 Vpp Single Ended Input		-39		dBc

AC Electrical Specification – CLK = 4GHz

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.4V; Clock: 4GHz, 0.4Vpp Differential; Differential Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
13.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.1Vpp SINGLE ENDED**						
13.1	Bandwidth	BW	-3dB Gain, 0.1 V_{PP} Single Ended Input		19		GHz
13.2	SFDR						
	60 MHz	SFDR	0.1 Vpp Single Ended Input		64		dBc
	4060 MHz	SFDR	0.1 Vpp Single Ended Input		64		dBc
	8060 MHz	SFDR	0.1 Vpp Single Ended Input		56		dBc
	12060 MHz	SFDR	0.1 Vpp Single Ended Input		46		dBc
	16060 MHz	SFDR	0.1 Vpp Single Ended Input		55		dBc
	20060 MHz	SFDR	0.1 Vpp Single Ended Input		51		dBc
13.3	THD						
	60 MHz	THD	0.1 Vpp Single Ended Input		-60		dBc
	4060 MHz	THD	0.1 Vpp Single Ended Input		-59		dBc
	8060 MHz	THD	0.1 Vpp Single Ended Input		-54		dBc
	12060 MHz	THD	0.1 Vpp Single Ended Input		-46		dBc
	16060 MHz	THD	0.1 Vpp Single Ended Input		-52		dBc
	20060 MHz	THD	0.1 Vpp Single Ended Input		-49		dBc
14.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.2Vpp SINGLE ENDED**						
14.1	Bandwidth	BW	-3dB Gain, 0.2 V_{PP} Single Ended Input		19		GHz
14.2	SFDR						
	60 MHz	SFDR	0.2 Vpp Single Ended Input		68		dBc
	4060 MHz	SFDR	0.2 Vpp Single Ended Input		59		dBc
	8060 MHz	SFDR	0.2 Vpp Single Ended Input		49		dBc
	12060 MHz	SFDR	0.2 Vpp Single Ended Input		40		dBc
	16060 MHz	SFDR	0.2 Vpp Single Ended Input		48		dBc
	20060 MHz	SFDR	0.2 Vpp Single Ended Input		45		dBc
14.3	THD						
	60 MHz	THD	0.2 Vpp Single Ended Input		-64		dBc
	4060 MHz	THD	0.2 Vpp Single Ended Input		-56		dBc
	8060 MHz	THD	0.2 Vpp Single Ended Input		-49		dBc
	12060 MHz	THD	0.2 Vpp Single Ended Input		-40		dBc
	16060 MHz	THD	0.2 Vpp Single Ended Input		-46		dBc
	20060 MHz	THD	0.2 Vpp Single Ended Input		-45		dBc
15.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.3Vpp SINGLE ENDED**						
15.1	Bandwidth	BW	-3dB Gain, 0.3 V_{PP} Single Ended Input		19		GHz
15.2	SFDR						
	60 MHz	SFDR	0.3 Vpp Single Ended Input		63		dBc
	4060 MHz	SFDR	0.3 Vpp Single Ended Input		54		dBc
	8060 MHz	SFDR	0.3 Vpp Single Ended Input		48		dBc
	12060 MHz	SFDR	0.3 Vpp Single Ended Input		37		dBc
	16060 MHz	SFDR	0.3 Vpp Single Ended Input		42		dBc
	20060 MHz	SFDR	0.3 Vpp Single Ended Input		40		dBc
15.3	THD						
	60 MHz	THD	0.3 Vpp Single Ended Input		-61		dBc
	4060 MHz	THD	0.3 Vpp Single Ended Input		-52		dBc
	8060 MHz	THD	0.3 Vpp Single Ended Input		-47		dBc
	12060 MHz	THD	0.3 Vpp Single Ended Input		-36		dBc
	16060 MHz	THD	0.3 Vpp Single Ended Input		-41		dBc
	20060 MHz	THD	0.3 Vpp Single Ended Input		-40		dBc

AC Electrical Specification

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
16.0	**TRACK TO HOLD SWITCHING AND HOLD STATE, TH1**						
16.1	Aperture Delay	ta	After V(CLK1P) - V(CLK1N) Goes Neg.		50		ps
16.2	Settling Time to 1 mV	ts	At Hold Capacitors. ttrack1,min Observed		70		ps
16.3	Diff. Droop Rate/V_{IN}		Initial Droop Rate		0.12		%/ns
17.0	**TRACK TO HOLD SWITCHING AND HOLD STATE, TH2**						
17.1	Aperture Delay	ta2	After V(CLK2P) - V(CLK2N) Goes Neg.		50		ps
17.2	Settling Time to 1 mV[1]	ts2	At DTH Output. ttrack2,min Observed		70		ps
17.3	Diff. Droop Rate/V_{IN}		Initial Droop Rate		0.12		%/ns

[1] Output is settled ta2 + ts2 after CLK2(P/N) downward transition.

Operating Conditions

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
18.0	**CLOCK INPUTS (CLK1P, CLK1N, CLK2P, CLK2N)**						
18.1	Amplitude	V_{CPP}		100	200	1000	mVpp
18.2	Common Mode Voltage	V_{CCM}		-250	0	250	mV
18.3	CLK1 Frequency	F_{CLK1}		1000		4000	MHz
18.4	CLK2 Frequency	F_{CLK2}		1000		4000	MHz
19.0	**ANALOG INPUT (INP, INN)**						
19.1	Full Scale Range	FSR	Differential			1000	mVpp
19.2	Common Mode Voltage	V_{CM}	When DC Coupled		-650		mV
20.0	**ANALOG OUTPUT (OUTP, OUTN)**						
20.1	Ext. Termination Voltage	V_{TERM}			0		V
20.2	Ext. Termination Resistor	R_{TERM}	Required From Outputs To Vterm		50		Ω
21.0	**POWER SUPPLY REQUIREMENTS**						
21.1	Negative Supply Voltage	VEE		-5.2	-5.4	-6.0	V
22.0	**OPERATING TEMPERATURE**[2]						
22.1	Case Temperature	Tc		-40		85	°C

[2] The part is designed to maintain high performance operation within a case temperature range of -40 ~ 85°C and we recommend not to exceed the Absolute Maximum Temperature shown on page 2. For the best performance, operation within the specified temperature range with proper heat dissipation is recommended. The metal pad where the part is soldered should be connected to the ground plane with thermal vias for better heat dissipation. A heatsink can be attached to the bottom of the PCB, on a metal pad connected to the metal pad where the part is soldered.

Pin Description and Pin Out (24 Lead QFP Package)

P/I/O	PIN	NUM.	NAME	FUNCTION
P	2, 4, 6, 10, 14, 16, 18, 20, 22, bottom plate	9	GND	Power Supply Ground
P	7, 13, 21, 23	4	VEE	Negative Power Supply
I	8	1	CLK1P	Clock 1 Input: High = TH1 in Track Mode Low = TH1 in Hold Mode
I	9	1	CLK1N	
I	11	1	CLK2P	Clock 2 Input: High = TH2 in Track Mode Low = TH2 in Hold Mode
I	12	1	CLK2N	
I	3	1	INP	Analog Input
I	5	1	INN	
O	17	1	OUTP	Analog Output
O	15	1	OUTN	
R	1, 19, 24	3	NC	Reserved

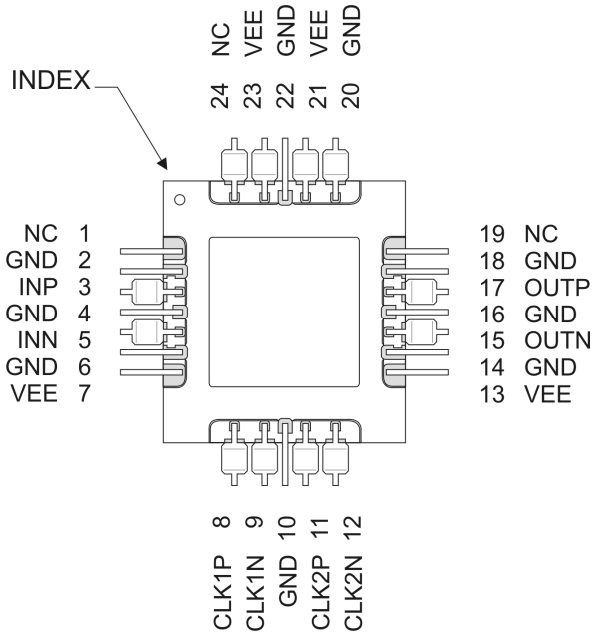

Figure 2 - RTH070 pinout (top view) 24 lead QFP package.

Definitions of Terms

Acquisition Time (tacq). The delay between the time a track-and-hold circuit (TH) enters track mode and the time the TH hold capacitor nodes track the input within some specified precision. The acquisition time sets a lower limit on the required track time during clocked operation.

Aperture Delay (ta). The average (or mean value) of the delay between the hold command (input clock switched from hold to track state) and the instant at which the analog input is sampled. The time is positive if the clock path delay is longer than the signal path delay. It is negative if the signal path delay is longer than the clock path delay.

Aperture Jitter (Δt). The standard deviation of the delay between the hold command (input clock switched from track-to-hold state) and the instant at which the analog input is sampled, excluding clock source jitter. It is the total jitter if the clock source is jitter free (ideal). Jitter diverges slowly as measurement time increases because of "1/f" noise, important at low frequencies (< 10 kHz). The specified jitter takes into account the white noise sources only (thermal and shot noise). For high-speed samplers this is reasonable, since even long data records span a time shorter than the time scale important for 1/f noise. For white-noise caused jitter, the clock and aperture jitter can be added in an rms manner to obtain the total sampling jitter.

Clock Jitter. The standard deviation of the mid-points of the relevant (rising or falling) edge of the clock source relative to the ideal edge (best fit). This jitter can be derived from the phase noise of the clock source, where the lower frequency bound of integration should correspond to the duration of a measurement record that the source will be used for.

Common-Mode Rejection Ratio (CMRR). Proportionality coefficient of the differential output and the common mode component of input signal. If an ideal symmetric input is available, CMR is the ratio of the differential output to the input on either input pin. A high-quality 50-ohm splitter may be used to generate the symmetrical inputs.

Full Scale Range (FSR). The maximum difference between the highest and lowest input levels for which various device performance specifications hold, unless otherwise noted.

Gain. Ratio of output signal magnitude to input signal magnitude. For sinewave inputs, it is the ratio of the amplitude of the first (main) harmonic output (HD1) to the amplitude of the input.

Input Bandwidth (BW). The input frequency at which the gain for sinewave input is reduced by 3 dB relative to its value at low frequencies. The low frequency range is defined as the range including DC over which the gain stays essentially constant. The high frequency range is characterized by an increase in gain variation versus frequency, at least including the eventual monotonic decrease of the gain ("roll-off"). The input bandwidth tends to be input amplitude dependent. It is normally largest for very small inputs and smallest for FSR inputs.

Settling Time (ts). The delay between the time that a track-and-hold circuit (TH) enters hold mode and the time that the TH hold capacitor nodes settle to within some specified precision. The settling time sets a lower limit on the required hold time during clocked operation.

Spurious Free Dynamic Range (SFDR). The ratio of the magnitude of the first (main) harmonic, HD1, and the highest other harmonic (or non-harmonic other tone, if present), as observed in the TH spectrum. The input is FSR, unless otherwise noted. SFDR in dB is given by 20log (SFDR as amplitude ratio), and is generally positive.

Total Harmonic Distortion (THD). The ratio of the square root of the sum of the harmonics 2 to 5 to the amplitude of the first (main) harmonic in the TH spectrum. THD in dB is given by 20log (THD as amplitude ratio), and is generally negative.

Theory of Operation

The RTH070 chip contains two TH's, TH1 and TH2, in series, together with clock shaping circuitry, BUFFER1 and BUFFER2, and a 50-ohm output driver, OUTBUF (Figure 1). To maximize dynamic range and insensitivity to noise, all non-DC internal circuits and all non-DC inputs and outputs are differential. TH1 determines the dynamic sampled-mode performance of the DTH. TH1 clock inputs, CLK1P and CLK1N, should be driven by a low-jitter clock source. TH2 is similar to TH1, except that its bandwidth requirement is lower.

The DTH receives a differential analog input signal at inputs INP and INN, which is sampled on the TH1 hold capacitors upon a falling transition of its differential clock voltage V(CLK1P) – V(CLK1N), after an aperture delay, ta, see Figure 3. TH1's aperture delay is positive, nominally 50ps.

The sampling instant is affected by clock source jitter (off-chip) and aperture jitter (caused by on-chip noise).

The held and buffered output of TH1, VTH1, is sampled on the TH2 hold capacitors upon a falling transition of its differential clock voltage V(CLK2P) – V(CLK2N), after an aperture delay closely equal to that of TH1. This allows simple out-of-phase clocking of TH1 and TH2 by having opposite phases for CLK1 and CLK2. Aperture jitter of TH2 is irrelevant, since the slew rate of the TH2 input is equal to the TH1 differential droop rate. TH2 can be in track mode before TH1 switches to hold, but a minimum track time of TH2 after TH1 enters hold mode must be observed to ensure that TH2 has fully acquired the TH1 output.

For out-of-phase clocking, the delay from the hold instant of TH1 to the ideal sampling time of circuitry after TH2 is close to one full clock cycle, for example 1 ns at a 1 GHz sampling rate, which eases the bandwidth requirement of subsequent circuitry. This is true, even though a small glitch will be present at the transition from track to hold of TH2. The output is accurate during the latter part of the clock cycle.

Lower limits for the sampling rates of TH1 and TH2 are set by single-ended hold-mode droop rates, and lead to the specification of maximum hold times. For longer hold times, the RTH070 must be allowed sufficient recovery time during track phase (or a sequence of track phases), so it can return to normal operation mode. The bandwidth of subsequent circuitry can be minimal if TH2 is clocked at its lowest recommended frequency.

Signal Descriptions

The RTH070 inputs are terminated on-chip with 50 Ω to GND. This automatically protects against off-chip high-impedance high-voltage disturbances. The absolute maximum rated voltage at input termination resistors is -1 V. The RTH070 is designed for 1 Vpp differential input signals. If operated in single-ended mode, the complementary input is self biased and can be left unconnected. Distortion in the single-ended mode will be higher than in differential mode, and differential input should be used for optimal performance. The INP and INN inputs are equivalent, except for the polarity of their effect on OUTP and OUTN.

All four clock input signals are terminated on-chip with 50 Ω to GND. Use differential clock signals for optimal performance. Large CLK1 edge rate benefits aperture jitter performance, small CLK1 and CLK2 amplitudes minimizes distortion due to clock feed-through in the higher clock frequency range. The RTH070 can also operate using single ended clocks. Distortion for single-ended clocks can be several dB higher than for differential clocks, and differential clocks should be used for optimal performance.

Due to its highly differential design, the RTH070 requires relatively modest power supply decoupling. The smaller decoupling capacitors from VEE to GND should be placed as close to the package as possible. Larger low frequency power supply decoupling capacitors, VEE to GND, should be placed within 1 inch of the RTH070. Depending on the expected noise on the supplies more capacitors in parallel may need to be used. With low-impedance supplies that are very quiet (no digital circuitry), the RTH070 can also perform well with no external decoupling at all.

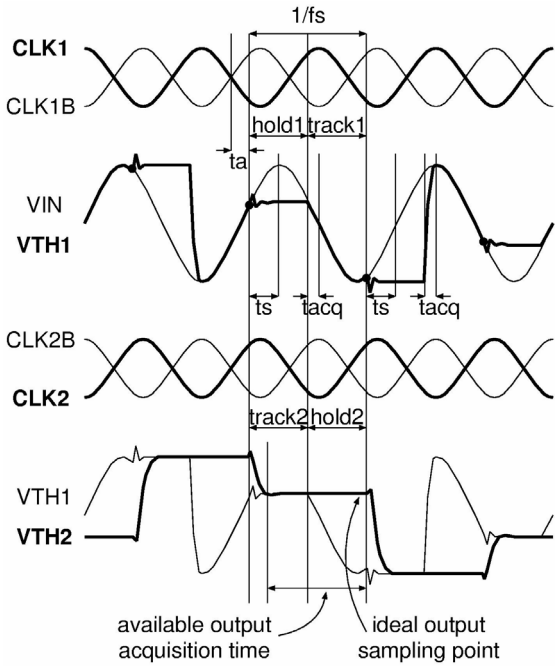

Figure 3 - Timing diagram for out-of-phase clocking of TH1 and TH2

Typical Operating Circuit

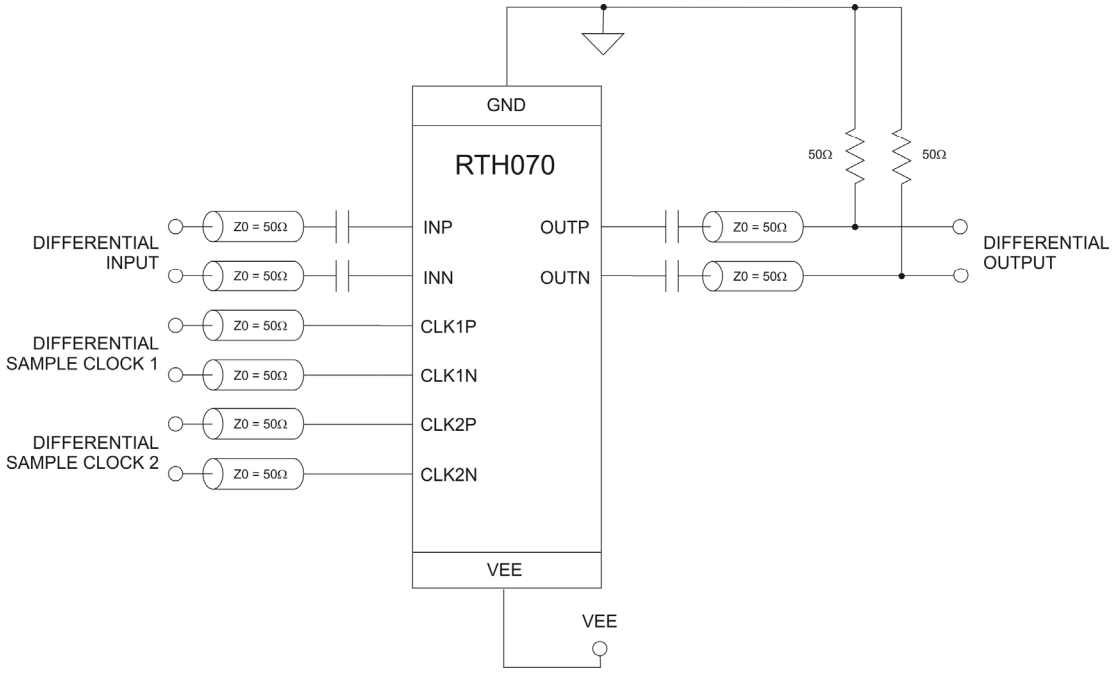

Figure 4 - Typical interface circuit. All differential inputs are terminated on-chip with 50 Ω to GND.

Typical Performance (CLK = 1GHz)

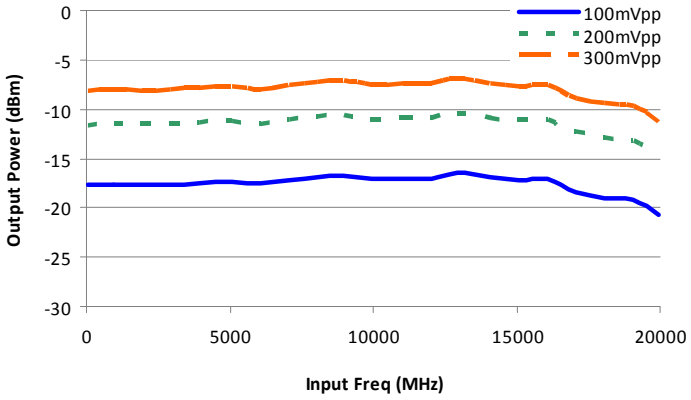

Figure 5 - Input Bandwidth, single ended input.

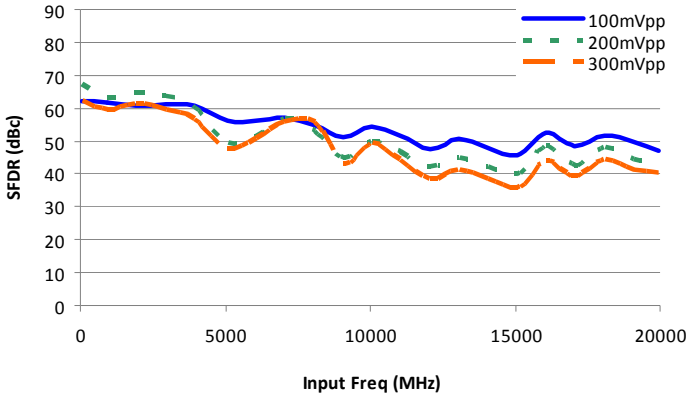

Figure 6 - SFDR x Fin, single tone, single ended input.

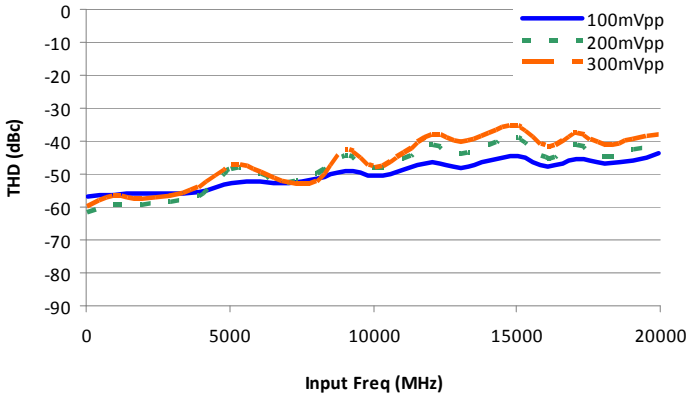

Figure 7 - THD x Fin, single tone, single ended input.

Typical Performance (CLK = 2GHz)

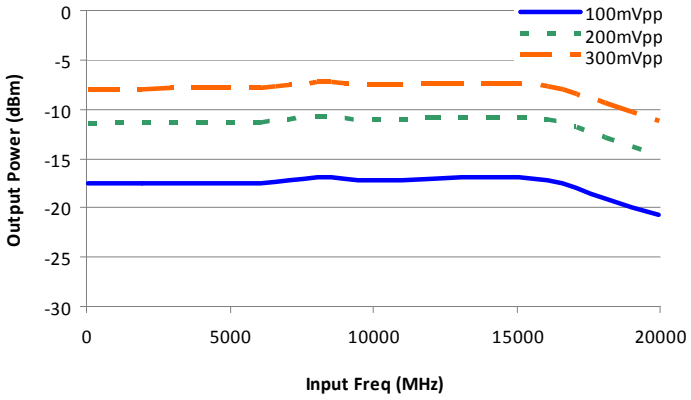

Figure 8 - Input Bandwidth, single ended input.

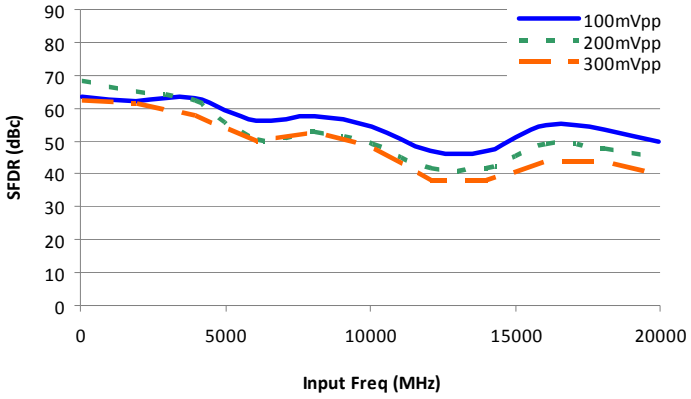

Figure 9 - SFDR x Fin, single tone, single ended input.

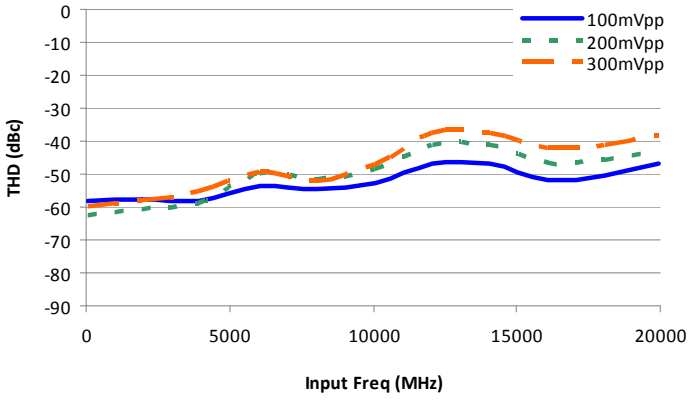

Figure 10 - THD x Fin, single tone, single ended input.

Typical Performance (CLK = 4GHz)

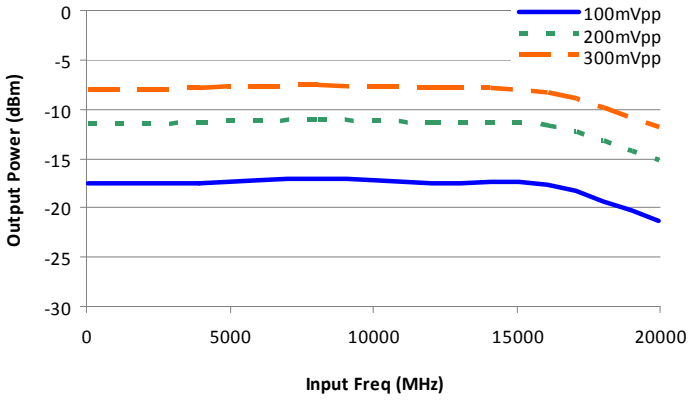

Figure 11 - Input Bandwidth, single ended input.

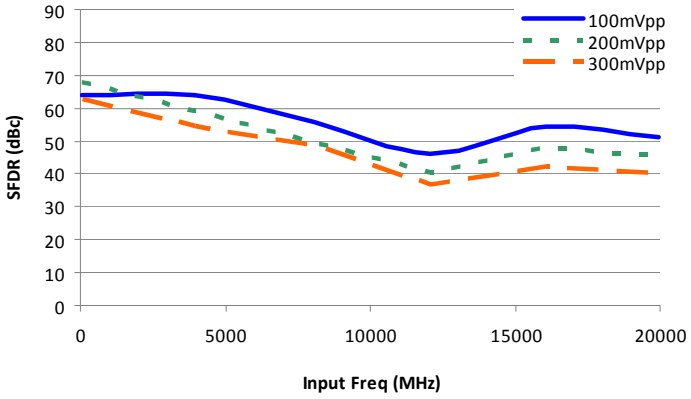

Figure 12 - SFDR x Fin, single tone, single ended input.

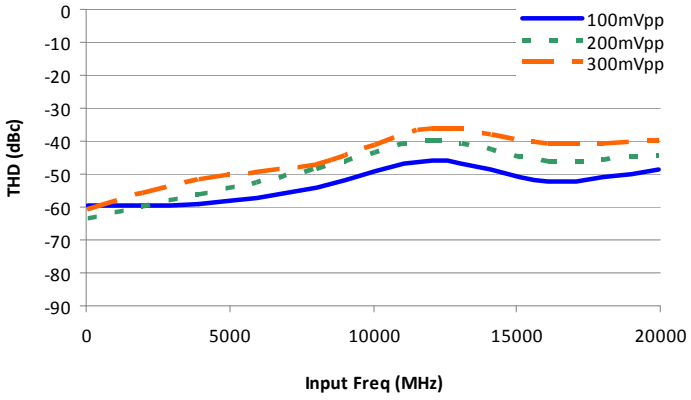

Figure 13 - THD x Fin, single tone, single ended input.

Package Information -HQ

The package is a high-speed 24 lead QFP with a Cu/Mo metal pad at the bottom.

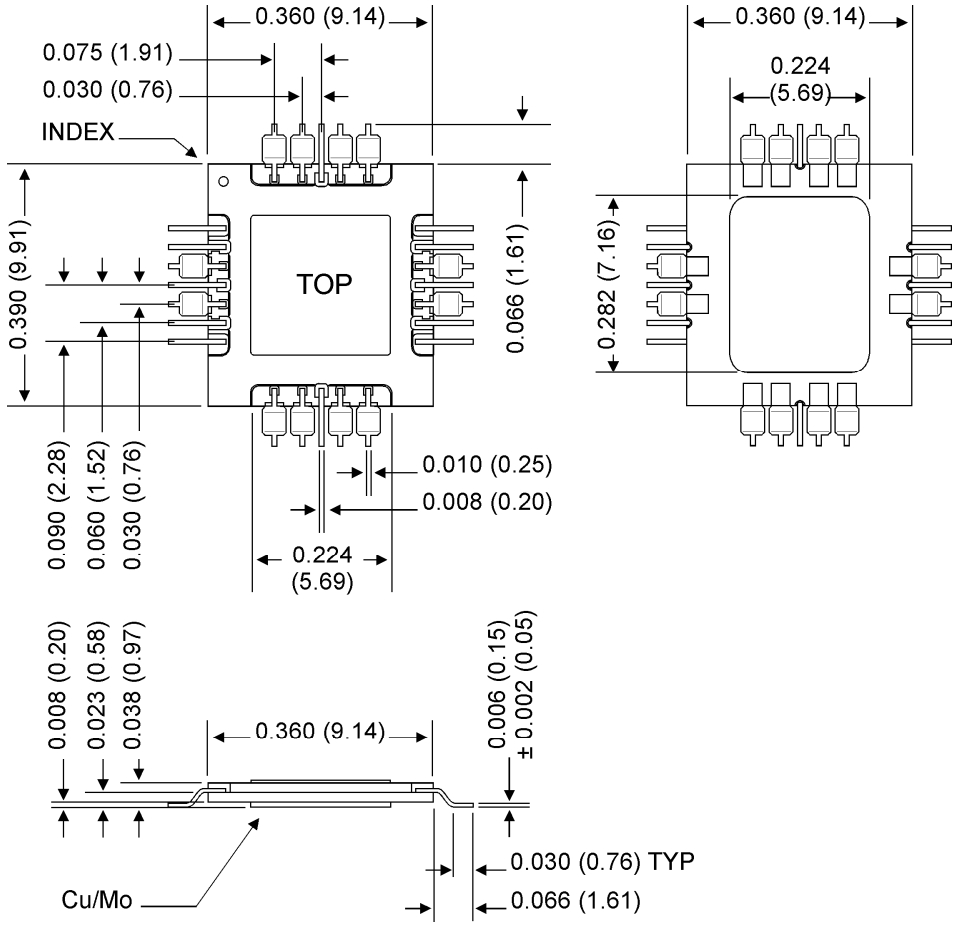

Figure 14 - RTH070-HQ package outline, dimensions in inches (mm).