TELEDYNE
SCIENTIFIC COMPANY

RTH110

50 GHz Bandwidth High Linearity Track-and-Hold

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RTH110

50 GHz Bandwidth High Linearity Track-and-Hold

Features

- 50 GHz Input Bandwidth
- Better than -40dBc THD up 30GHz and -35dBc up to 50GHz
- Better than 40dBc SFDR up to 30GHz and 35dBc up to 50GHz
- 100 to 1,000 MHz Sampling Rate
- Differential Analog Input/Output
- Output Clock
- 1.9W Power Dissipation
- Single Power Supply
- QFN Package

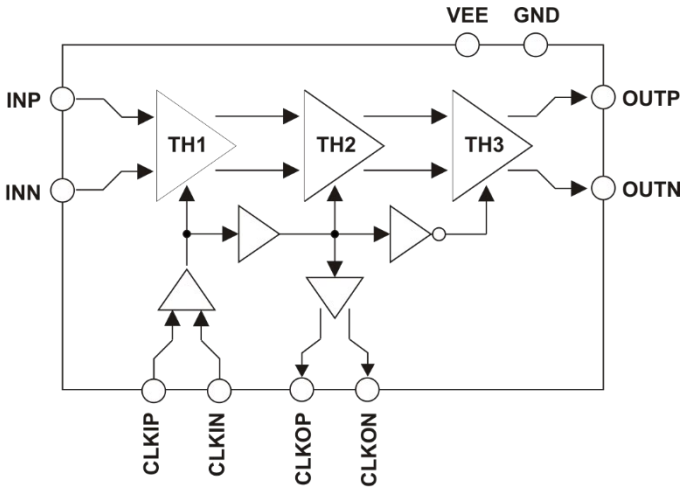

Figure 1 - Functional Block Diagram

Product Description

RTH110's bandwidth and aperture jitter enable accurate sampling of DC to multi-GHz signals. The differential-to-differential track-and-hold cascades three track-and-hold circuits, TH1, TH2, and TH3. TH1 capture the input signal and TH2/TH3 provide a longer sampling time for the subsequent circuit. The requirement of only one clock and the fact the RTH110 provides an output clock, eases the clock distribution for the sampling and digitizing circuitry relative to the case of a track-and-hold (TH) with dual clocks.

Ordering information

PART NUMBER	DESCRIPTION
RTH110-QN	20 I/O QFN Package
RTH110-DI	Die
EVRTH110	Evaluation Board

CAUTION
DEVICE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)

Absolute Maximum Ratings

Supply Voltages

VEE to GND ……..……..…..-5.5V

Input Voltages

INP, INN to GND …..……..……-1V
CLK1P, CLK1N, CLK2P, CLK2N to GND ……..….. -1V

Temperature

Case Temperature ……..……..…..+125°C
Junction Temperature ……..….. +150°C
Lead, Soldering (10 Seconds) …….. +220°C
Storage ……..…… -40 to 125°C

DC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.2V; Clock: 100MHz, 0.4Vpp Differential; Input: 300mV Differential; Differential Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
1.0	**DC TRANSFER FUNCTION**						
1.1	Gain	G			0		dB
2.0	**ANALOG INPUT (INP, INN)**						
2.1	Common Mode Voltage	IN_{CM}	Self Bias		0		mV
2.2	Input Impedance	R_{IIN}	Each Lead to GND		50		Ω
3.0	**CLOCK INPUT (CLKIP, CLKIN)**						
3.1	Input Resistance	R_{CIN}	Each Lead to GND		50		Ω
4.0	**ANALOG OUTPUT (OUTP, OUTN)**						
4.1	Output Resistance	R_{OUT}	Each Output to GND		1000		Ω
4.2	Maximum Current		Into Output Lead			20	mA
4.3	Output Offset Voltage	V_{OFF}	Absolute Value (No Input Signal)		25		mV
4.4	Common Mode Voltage	OUT_{CM}	Outputs Terminated 50Ω to GND		-0.55		V
5.0	**POWER SUPPLY REQUIREMENTS**						
5.1	Negative Supply Current	IEE			360		mA
5.2	Power Dissipation	P			1.9		W

AC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.2V; Clock: 100MHz, 0.4Vpp Differential; Input: 300mV Differential; Differential Outputs Terminated Into 50 Ω to 0V.

6.0	DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.3Vpp DIFFERENTIAL						
6.1	Bandwidth	BW	-3dB Gain, 0.3 V_{PP} Differential Input	47	50		GHz
	SFDR						
	20 MHz	SFDR	0.3 Vpp Differential Input				dBc
	2020 MHz	SFDR	0.3 Vpp Differential Input		53		dBc
	4020 MHz	SFDR	0.3 Vpp Differential Input		49		dBc
	6020 MHz	SFDR	0.3 Vpp Differential Input		48		dBc
	8020 MHz	SFDR	0.3 Vpp Differential Input		48		dBc
	10020 MHz	SFDR	0.3 Vpp Differential Input		50		dBc
	12020 MHz	SFDR	0.3 Vpp Differential Input		50		dBc
	14020 MHz	SFDR	0.3 Vpp Differential Input		49		dBc
	16020 MHz	SFDR	0.3 Vpp Differential Input		47		dBc
	18020 MHz	SFDR	0.3 Vpp Differential Input		46		dBc
	20020 MHz	SFDR	0.3 Vpp Differential Input		44		dBc
	22020 MHz	SFDR	0.3 Vpp Differential Input		47		dBc
6.2	24020 MHz	SFDR	0.3 Vpp Differential Input		46		dBc
	26020 MHz	SFDR	0.3 Vpp Differential Input		44		dBc
	28020 MHz	SFDR	0.3 Vpp Differential Input		41		dBc
	30020 MHz	SFDR	0.3 Vpp Differential Input		42		dBc
	32020 MHz	SFDR	0.3 Vpp Differential Input		41		dBc
	34020 MHz	SFDR	0.3 Vpp Differential Input		41		dBc
	36020 MHz	SFDR	0.3 Vpp Differential Input		42		dBc
	38020 MHz	SFDR	0.3 Vpp Differential Input		39		dBc
	40020 MHz	SFDR	0.3 Vpp Differential Input		41		dBc
	42020 MHz	SFDR	0.3 Vpp Differential Input		41		dBc
	44020 MHz	SFDR	0.3 Vpp Differential Input		39		dBc
	46020 MHz	SFDR	0.3 Vpp Differential Input		38		dBc
	48020 MHz	SFDR	0.3 Vpp Differential Input		37		dBc
	50020 MHz	SFDR	0.3 Vpp Differential Input		38		dBc
	20 MHz	THD	0.3 Vpp Differential Input				dBc
	2020 MHz	THD	0.3 Vpp Differential Input		-54		dBc
	4020 MHz	THD	0.3 Vpp Differential Input		-48		dBc
	6020 MHz	THD	0.3 Vpp Differential Input		-48		dBc
	8020 MHz	THD	0.3 Vpp Differential Input		-47		dBc
	10020 MHz	THD	0.3 Vpp Differential Input		-48		dBc
	12020 MHz	THD	0.3 Vpp Differential Input		-49		dBc
6.3	14020 MHz	THD	0.3 Vpp Differential Input		-48		dBc
	16020 MHz	THD	0.3 Vpp Differential Input		-50		dBc
	18020 MHz	THD	0.3 Vpp Differential Input		-46		dBc
	20020 MHz	THD	0.3 Vpp Differential Input		-43		dBc
	22020 MHz	THD	0.3 Vpp Differential Input		-45		dBc
	24020 MHz	THD	0.3 Vpp Differential Input		-46		dBc
	26020 MHz	THD	0.3 Vpp Differential Input		-43		dBc
	28020 MHz	THD	0.3 Vpp Differential Input		-41		dBc
	30020 MHz	THD	0.3 Vpp Differential Input		-41		dBc
	32020 MHz	THD	0.3 Vpp Differential Input		-42		dBc
	34020 MHz	THD	0.3 Vpp Differential Input		-42		dBc
	36020 MHz	THD	0.3 Vpp Differential Input		-42		dBc
	38020 MHz	THD	0.3 Vpp Differential Input		-42		dBc
	40020 MHz	THD	0.3 Vpp Differential Input		-41		dBc
	42020 MHz	THD	0.3 Vpp Differential Input		-42		dBc
	44020 MHz	THD	0.3 Vpp Differential Input		-41		dBc
	46020 MHz	THD	0.3 Vpp Differential Input		-36		dBc
	48020 MHz	THD	0.3 Vpp Differential Input		-37		dBc
	50020 MHz	THD	0.3 Vpp Differential Input		-38		dBc

AC Electrical Specification

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
7.0	**TRACK TO HOLD SWITCHING AND HOLD STATE, TH1**						
7.1	Aperture Delay	ta	After V(CLKIP) - V(CLKIN) Goes Neg.				ps
8.0	**TRACK TO HOLD SWITCHING AND HOLD STATE, TH3**						
8.1	Settling Time to 1 mV	ts	At Output. Min Observed				ps
8.2	Diff. Droop Rate/V_{IN}		Initial Droop Rate				%/ns
8.3	Maximum Hold Time	$t_{HD,MAX}$					ns

Operating Conditions

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
9.0	**CLOCK INPUTS (CLKIP, CLKIN)**						
9.1	Amplitude	V_{CPP}	Differential		600		mVpp
9.2	Common Mode Voltage	V_{CCM}			0		mV
9.3	CLKI Frequency	F_{CLK1}		100		1,000	MHz
9.4	Rise and Fall Time	T_{RF}			150		ps
10.0	**CLOCK OUTPUTS (CLKOP, CLKON)**						
10.1	Amplitude	V_{COPP}	Single End With 50Ω Termination		300		mVpp
10.2	Ext. Termination Voltage	V_{TERM}				2	V
11.0	**ANALOG INPUT (INP, INN)**						
11.1	Full Scale Range	FSR	Differential			1000	mVpp
11.2	Common Mode Voltage	V_{CM}	When DC Coupled		0		mV
12.0	**ANALOG OUTPUT (OUTP, OUTN)**						
12.1	Ext. Termination Resistor	R_{TOUT}	Required From Outputs To GND		50		Ω
13.0	**POWER SUPPLY REQUIREMENTS**						
13.1	Negative Supply Voltage	VEE		-5.0	-5.2	-5.4	V
14.0	**OPERATING TEMPERATURE**[1]						
14.1	Case Temperature	Tc		-40		85	°C

[1] The part is designed to maintain high performance operation within a case temperature range of -40 ~ 85°C and we recommend not to exceed the Absolute Maximum Temperature shown on page 2. For the best performance, operation within the specified temperature range with proper heat dissipation is recommended. The metal pad where the part is soldered should be connected to the ground plane with thermal vias for better heat dissipation. A heatsink can be attached to the bottom of the PCB, on a metal pad connected to the metal pad where the part is soldered.

Pin Description and Pin Out (20 I/O QFN Package)

P/I/O	PIN	NUM.	NAME	FUNCTION
P	1,3,5,8,11,13,15,18, bottom pad	8	GND	Power Supply Ground
P	17,19	2	VEE	Negative Power Supply
I	7	1	CLKIP	Clock Input: High = TH1 in Track Mode
I	6	1	CLKIN	Low = TH1 in Hold Mode
O	10	1	CLKOP	Clock Output
O	9	1	CLKON	
I	2	1	INP	Analog Input
I	4	1	INN	
O	12	1	OUTP	Analog Output
O	14	1	OUTN	
C	16	1	TSEN	Temperature Sensor
C	20	1	CCAL	Control

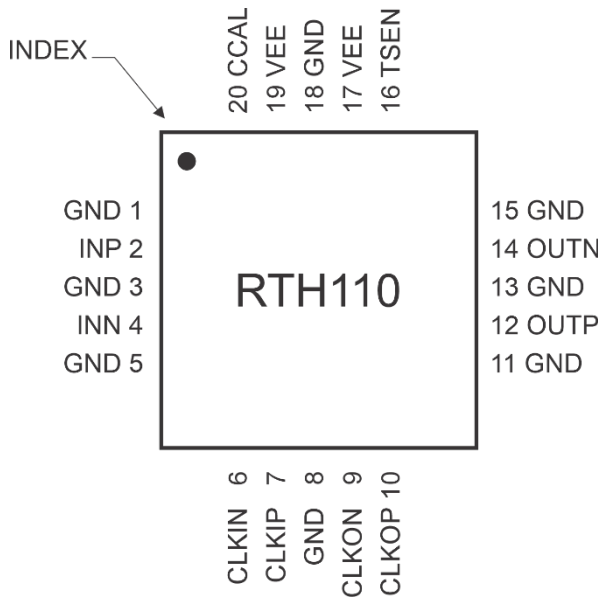

Figure 2 – RTH110 pinout (top view) 20 I/O QFN package.

Definitions of Terms

Acquisition Time (tacq). The delay between the time a track-and-hold circuit (TH) enters track mode and the time the TH hold capacitor nodes track the input within some specified precision. The acquisition time sets a lower limit on the required track time during clocked operation.

Aperture Delay (ta). The average (or mean value) of the delay between the hold command (input clock switched from hold to track state) and the instant at which the analog input is sampled. The time is positive if the clock path delay is longer than the signal path delay. It is negative if the signal path delay is longer than the clock path delay.

Aperture Jitter (Δt). The standard deviation of the delay between the hold command (input clock switched from track-to-hold state) and the instant at which the analog input is sampled, excluding clock source jitter. It is the total jitter if the clock source is jitter free (ideal). Jitter diverges slowly as measurement time increases because of "1/f" noise, important at low frequencies (< 10 kHz). The specified jitter takes into account the white noise sources only (thermal and shot noise). For high-speed samplers this is reasonable, since even long data records span a time shorter than the time scale important for 1/f noise. For white-noise caused jitter, the clock and aperture jitter can be added in an rms manner to obtain the total sampling jitter.

Clock Jitter. The standard deviation of the mid-points of the relevant (rising or falling) edge of the clock source relative to the ideal edge (best fit). This jitter can be derived from the phase noise of the clock source, where the lower frequency bound of integration should correspond to the duration of a measurement record that the source will be used for.

Common-Mode Rejection Ratio (CMRR). Proportionality coefficient of the differential output and the common mode component of input signal. If an ideal symmetric input is available, CMR is the ratio of the differential output to the input on either input pin. A high-quality 50-ohm splitter may be used to generate the symmetrical inputs.

Full Scale Range (FSR). The maximum difference between the highest and lowest input levels for which various device performance specifications hold, unless otherwise noted.

Gain. Ratio of output signal magnitude to input signal magnitude. For sinewave inputs, it is the ratio of the amplitude of the first (main) harmonic output (HD1) to the amplitude of the input.

Input Bandwidth (BW). The input frequency at which the gain for sinewave input is reduced by 3 dB relative to its value at low frequencies. The low frequency range is defined as the range including DC over which the gain stays essentially constant. The high frequency range is characterized by an increase in gain variation versus frequency, at least including the eventual monotonic decrease of the gain ("roll-off"). The input bandwidth tends to be input amplitude dependent. It is normally largest for very small inputs and smallest for FSR inputs.

Settling Time (ts). The delay between the time that a track-and-hold circuit (TH) enters hold mode and the time that the TH hold capacitor nodes settle to within some specified precision. The settling time sets a lower limit on the required hold time during clocked operation.

Spurious Free Dynamic Range (SFDR). The ratio of the magnitude of the first (main) harmonic, HD1, and the highest other harmonic (or non-harmonic other tone, if present), as observed in the TH spectrum. The input is FSR, unless otherwise noted. SFDR in dB is given by 20log (SFDR as amplitude ratio), and is generally positive.

Total Harmonic Distortion (THD). The ratio of the square root of the sum of the harmonics 2 to 5 to the amplitude of the first (main) harmonic in the TH spectrum. THD in dB is given by 20log (THD as amplitude ratio), and is generally negative.

Theory of Operation

The RTH110 contains three TH's, TH1, TH2 and TH3, in series, together with clock shaping circuitry, and a 50-ohm output driver. To maximize dynamic range and insensitivity to noise, all non-DC internal circuits and all non-DC inputs and outputs are differential. TH1 determines the dynamic sampled-mode performance of the Track and Hold. TH1 clock inputs, CLKIP and CLKIN, should be driven by a low-jitter clock source. TH2 and TH3 get their clocks from TH1 clock input.

The Track and Hold receives a differential analog input signal at inputs INP and INN, which is sampled on the TH1 hold capacitors upon a falling transition of its differential clock voltage V(CLKIP) – V(CLKIN), after an aperture delay, ta. The sampling instant is affected by clock source jitter (off-chip) and aperture jitter (caused by on-chip noise).

The held and buffered output of TH1, VTH1, is sampled on the TH2 hold capacitors after a fixed delay. The output of TH2, VTH2 is then sampled by TH3. TH3 clock have the opposite phase of the TH2 clock. Aperture jitter of TH2 and TH3 is irrelevant, since TH1 will be in hold mode when TH2 capture the signal, and in similar fashion TH3 will capture the hold mode signal of TH2.

Since the clocks for TH2 and TH3 are generated internally only one clock source is need. An image of the TH2 clock is available externally. This clock can be used to drive the clock of subsequent circuit such as an ADC.

Signal Descriptions

The RTH110 inputs are terminated on-chip with equivalent 50Ω impedance to GND. This automatically protects against off-chip high-impedance high-voltage disturbances. The absolute maximum rated voltage at input termination resistors is -1 V. The RTH110 is designed for 1 Vpp differential input signals. If operated in single-ended mode, the complementary input needs to be terminated to ground with 50Ω. Distortion in the single-ended mode will be higher than in differential mode, and differential input should be used for optimal performance. The INP and INN inputs are equivalent, except for the polarity of their effect on OUTP and OUTN.

Both clock input signals are terminated on-chip with 50Ω to GND. Use differential clock signals for optimal performance. Large CLKI edge rate benefits aperture jitter performance, small CLKI amplitudes minimizes distortion due to clock feed-through in the higher clock frequency range. The RTH110 can also operate using single ended clocks. Distortion for single-ended clocks can be several dB higher than for differential clocks, and differential clocks should be used for optimal performance.

Due to its highly differential design, the RTH110 requires relatively modest power supply decoupling. The smaller decoupling capacitors from VEE to GND should be placed as close to the package as possible. Larger low frequency power supply decoupling capacitors, VEE to GND, should be placed within 1 inch of the RTH110. Depending on the expected noise on the supplies more capacitors in parallel may need to be used. With low-impedance supplies that are very quiet (no digital circuitry), the RTH110 can also perform well with no external decoupling at all.

Typical Operating Circuit

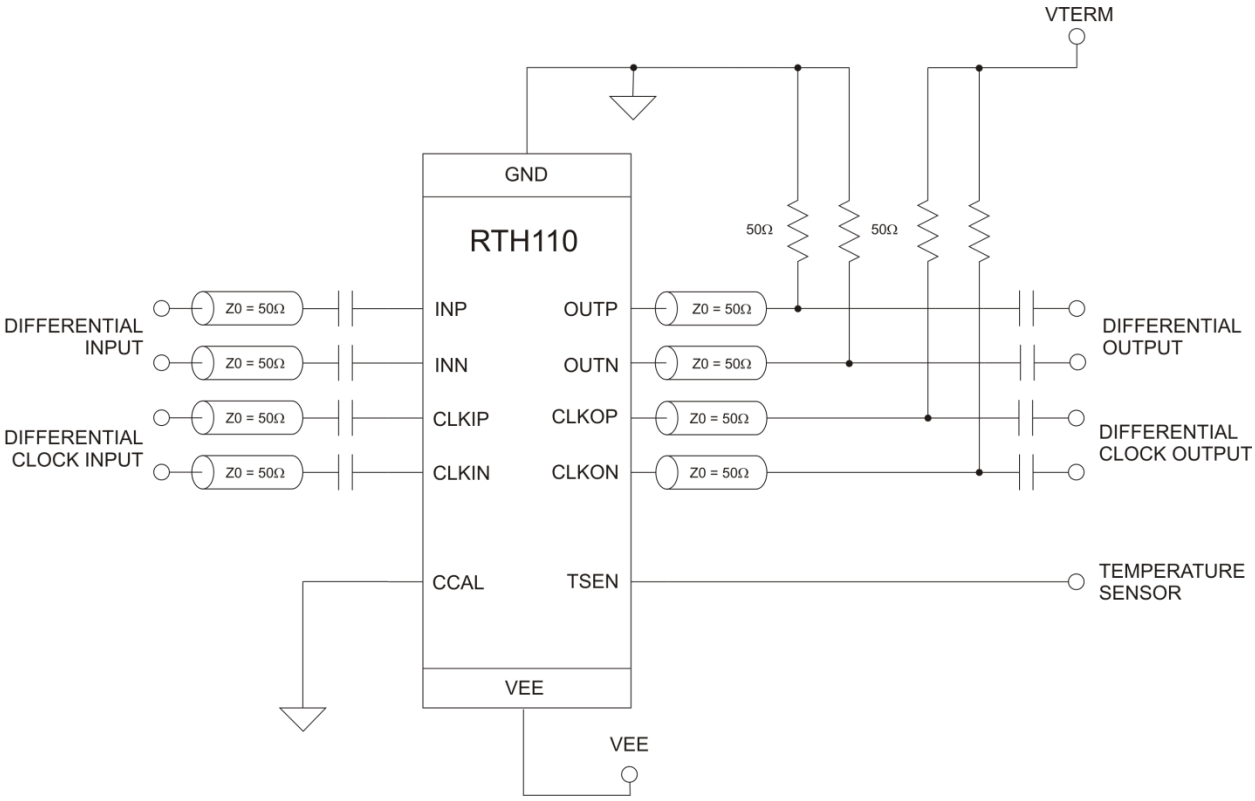

Figure 3 - Typical operating circuit.

Output Clock Interface

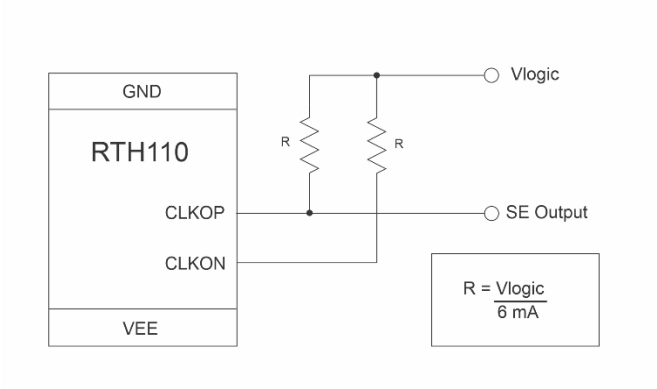

Figure 4 – Single Ended logic interface.

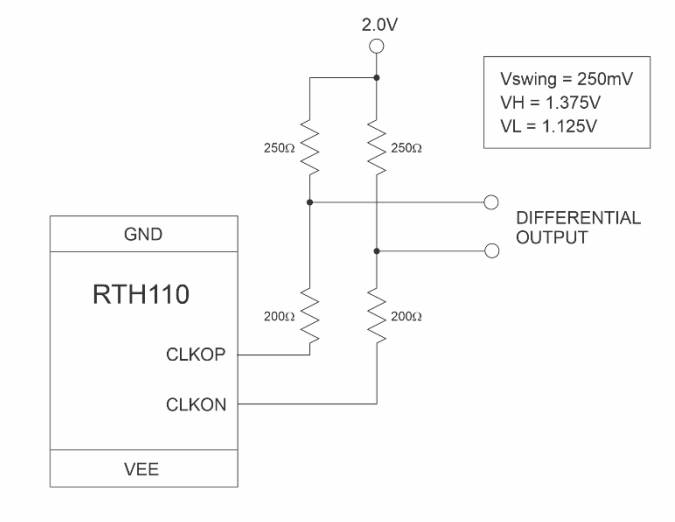

Figure 5 – Differential interface to LVDS (100 Ohm termination at destination).

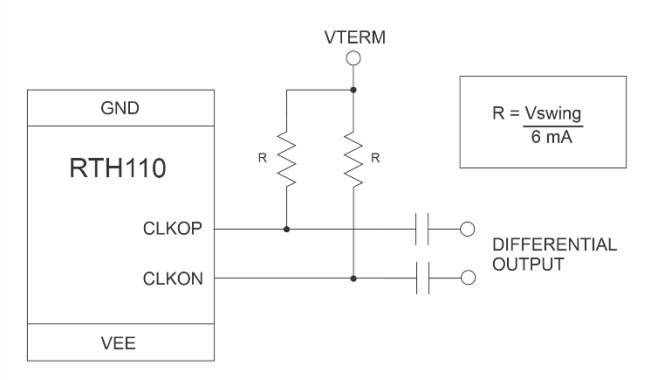

Figure 6 – Differential interface.

Equivalent Circuit

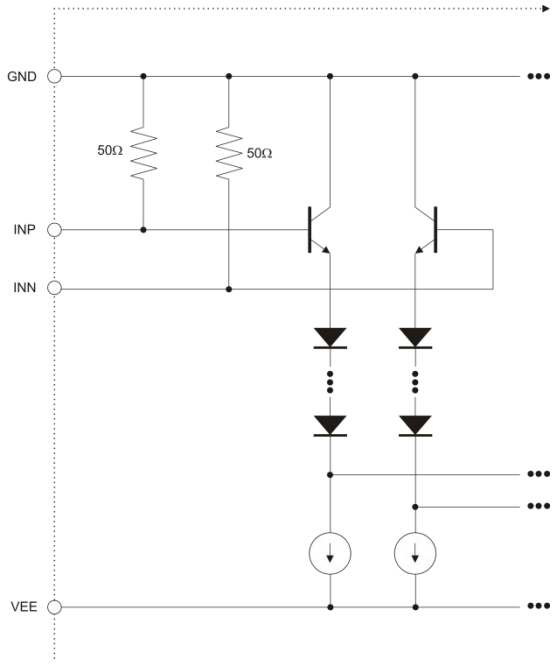

Figure 7 - Input circuit.

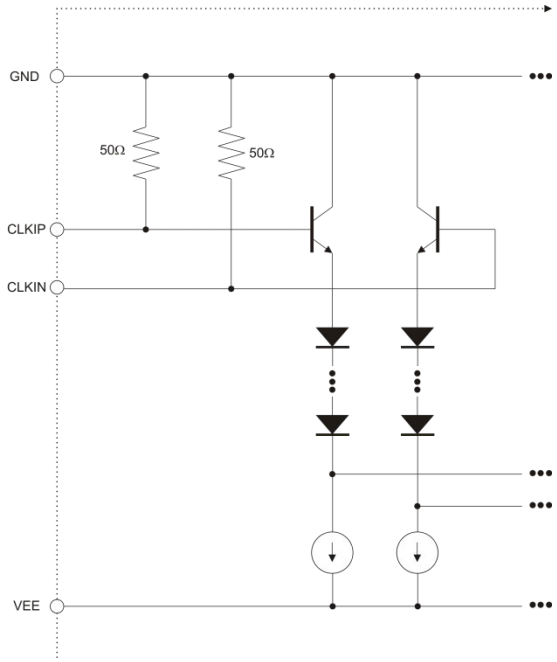

Figure 8- Clock Input circuit.

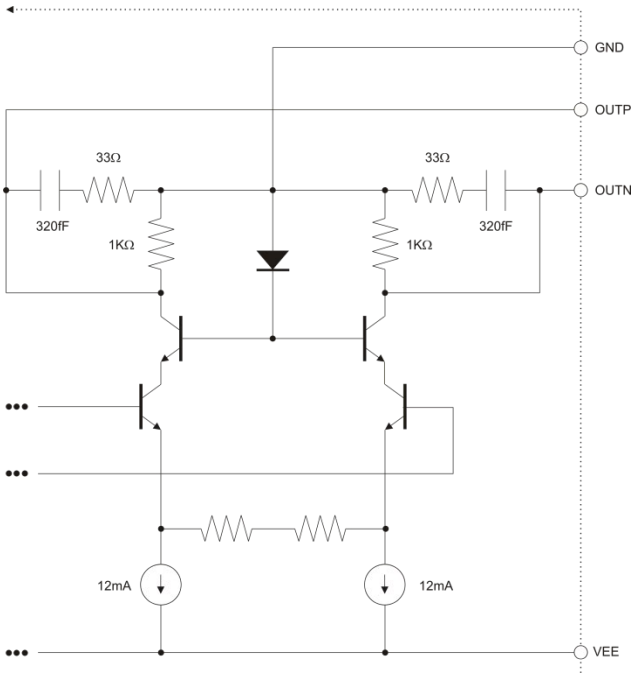

Figure 9- Output circuit.

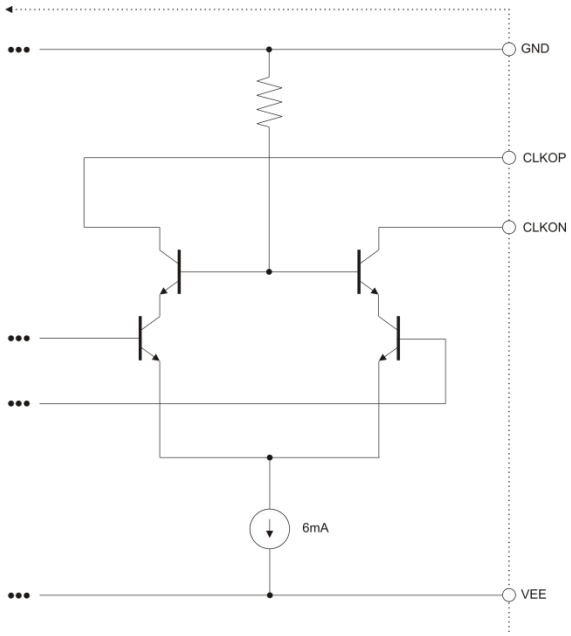

Figure 10 - Clock Output circuit.

Typical Performance 100MHz Clock, 300mVpp Differential Input

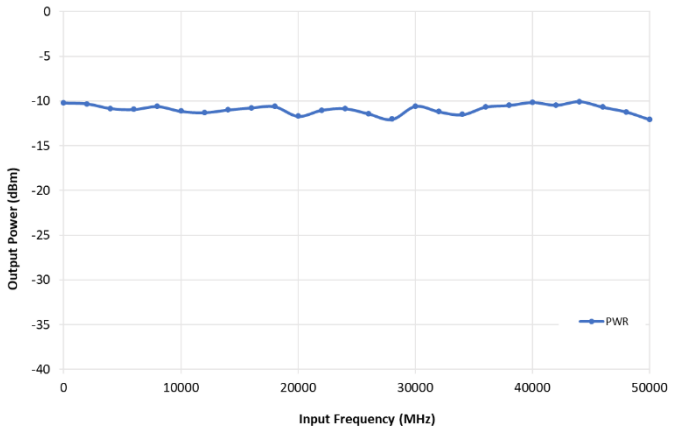

Figure 11 - Input Bandwidth.

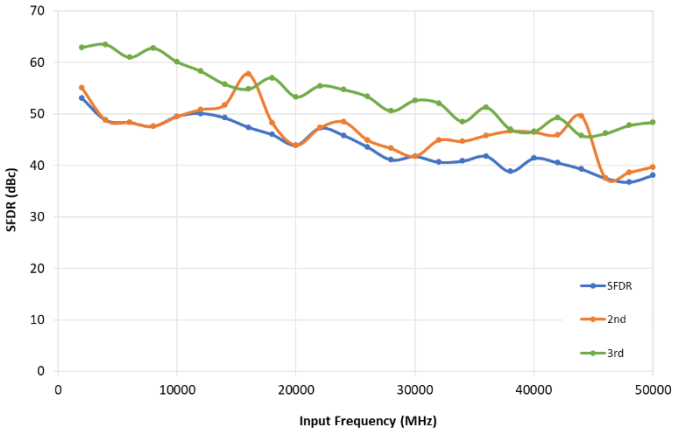

Figure 12 - SFDR x Fin, single tone.

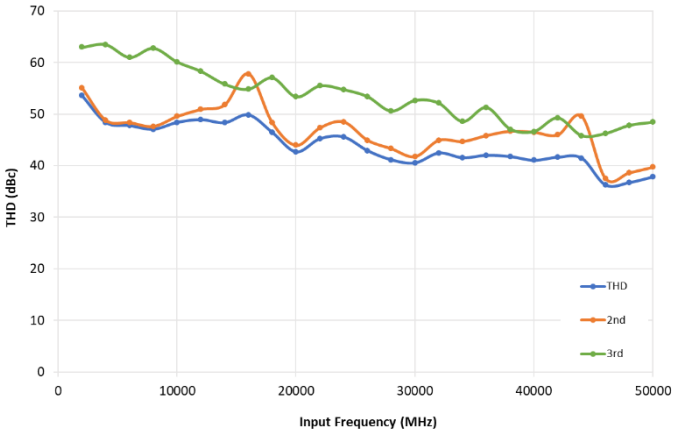

Figure 13 - THD x Fin, single tone.

Typical Performance 500MHz Clock, 400mVpp Differential Input

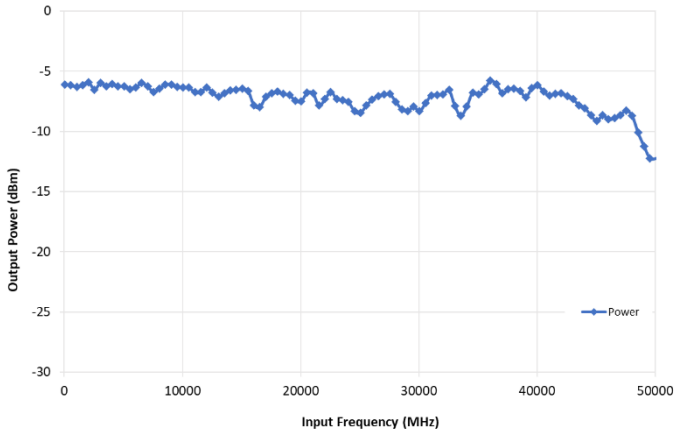

Figure 14 - Input Bandwidth.

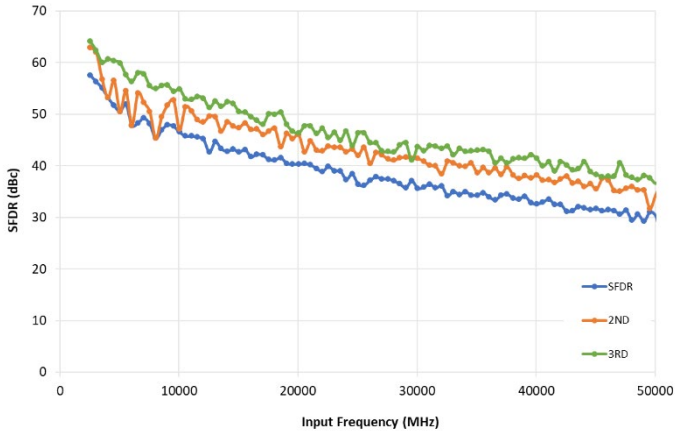

Figure 15 - SFDR x Fin, single tone.

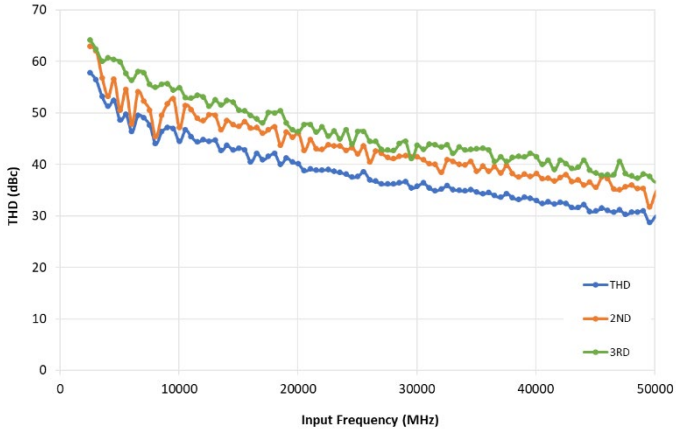

Figure 16 - THD x Fin, single tone.

Typical Performance 800MHz Clock, 400mVpp Differential Input

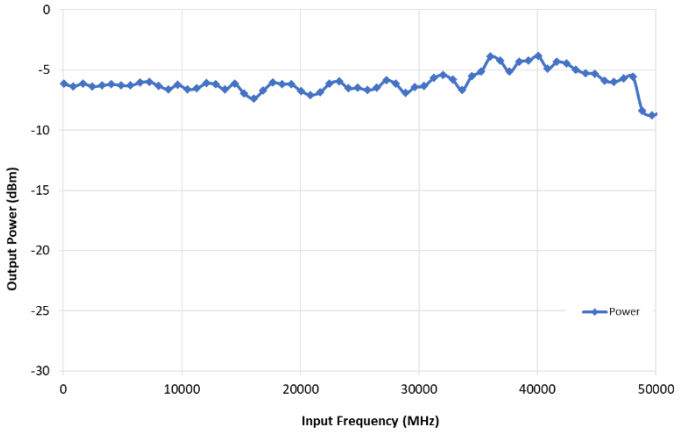

Figure 17 - Input Bandwidth.

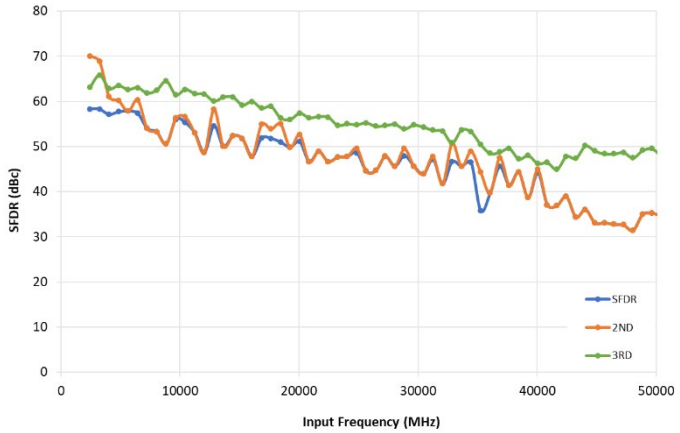

Figure 18 - SFDR x Fin, single tone.

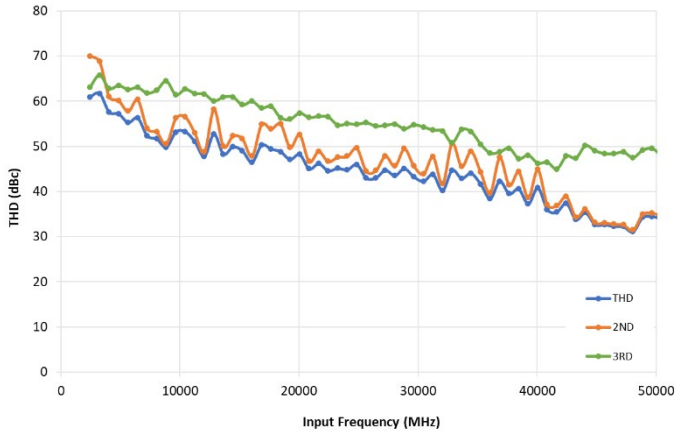

Figure 19 - THD x Fin, single tone.

Package Information -QN

The package is an organic laminate 20 IO QFN. Thermal resistance (junction to bottom of the case) is 5 C/W.

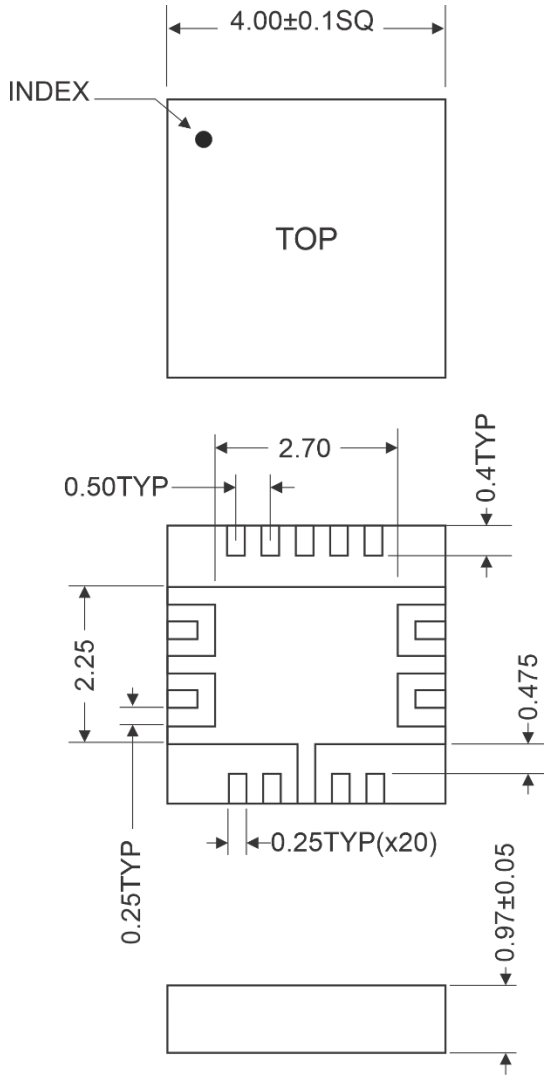

Figure 20 – RTH110-QN package outline, dimensions in mm.