

TPG002

9ps CML Driver With Integrated 43GHz Track-and-Hold

Features

- High Bandwidth CML Driver with Adjustable Output Amplitude
- 9 ps Maximum Rise/Fall Time CML Driver
- 43 GHz Input Bandwidth Integrated
 Track and Hold
- Better than -40dBc THD Over the Total Bandwidth with Small Signal Input
- Better than 35dBc SFDR Over the Total Bandwidth with Small Signal Input
- 50 300 MHz Sampling Rate
- Differential Analog Input/Output
- ♦ Output Held more than Half Clock Cycle
- ♦ 2W Power Dissipation
- Single Power Supply
- Adjustable Track and Hold Output Common Mode

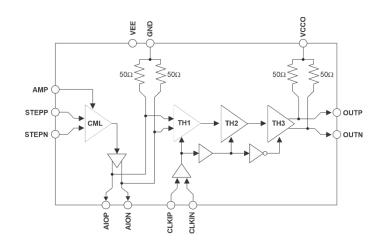


Figure 1 - Functional Block Diagram

Product Description

The TPG002 is comprised of a CML driver and a track and hold amplifier. The CML driver can be used to generate a step signal that is captured, along with any reflections in the AIO line, by the track and hold. The Track-and-hold cascades three track-and-hold circuits: TH1, TH2 and

TH3. It provides an output held for more than half a clock cycle, easing bandwidth requirements of subsequent circuitry relative to the case of a single track-and-hold (TH). The requirement of only one clock source simplifies the clock distribution design.

Ordering information

PART NUMBER	DESCRIPTION	
TPG002-QN	20 I/O QFN Package	CAUTION
TPG002-DI	Die	DEVICE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)
EVTPG002	Evaluation Board	DISCHARGE (ESD)



Pin Description and Pin Out (20 I/O QFN Package)

P/I/O	PIN	NUM.	NAME	FUNCTION	
Р	1,3,5,8,11,13,15, bottom pad	8	GND	Power Supply Ground	
Р	18	1	VEETH	Negative Power Supply – Track and Hold	
Р	19	1	VEED	Negative Power Supply – CML Driver	
ı	10	1	CLKIP	Clock Input: High = TH1 in Track Mode	
ı	9	1	CLKIN	Low = TH1 in Hold Mode	
ı	7	1	STEPP	CMI Driver Input	
ı	6	1	STEPN	CML Driver Input	
ı	2	1	AIOP	Analog Innut/Outnut	
I	4	1	AION	Analog Input/Output	
0	12	1	OUTP	Analog Output	
0	14	1	OUTN	Analog Output	
С	16	1	TSEN	Temperature Sensor	
Р	16	1	VTERM	Output Termination Voltage	
С	20	1	DRVGC	CML Output Gain Control	

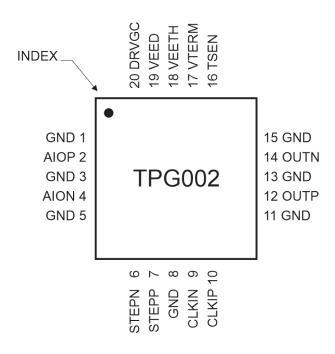


Figure 2 - TPG002 pinout (top view) 20 I/O QFN package.



Typical Operating Circuit

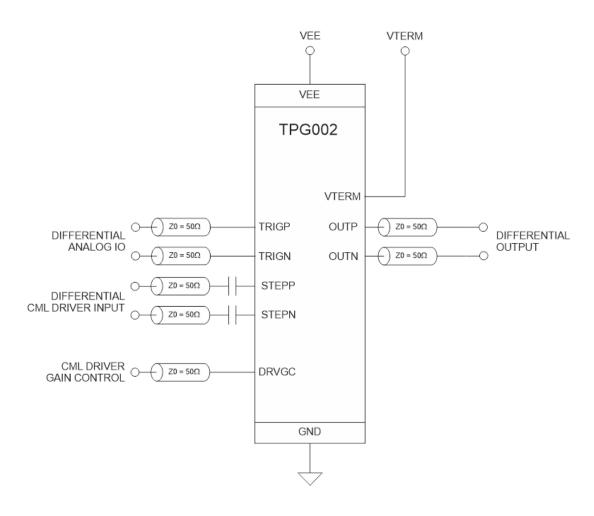


Figure 3 - Typical operating circuit.



Package Information -QN

The package is an organic laminate 20 IO QFN.

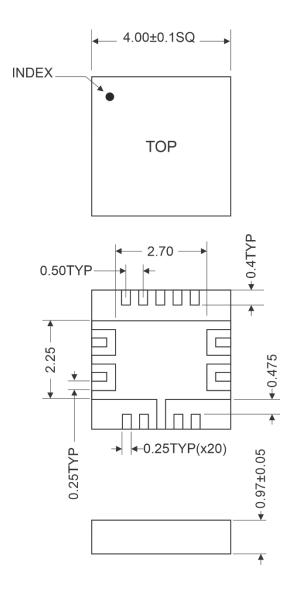


Figure 14 - TPG002-QN package outline, dimensions in mm.