TELEDYNE
SCIENTIFIC COMPANY

RTH122

24 GHz Bandwidth High Linearity Track-and-Hold

REV-DATE PA2-4923
FILE DS_0202PA2-4923

DS

RTH122

24 GHz Bandwidth High Linearity Track-and-Hold

Features

- 24 GHz Input Bandwidth
- -45 dBc THD with Fin = 3 GHz, 1 Vpp Diff
- -35 dBc THD with Fin = 5 GHz, 1 Vpp Diff
- 1000 - 4000 MHz Sampling Rate
- Differential Analog Input/Output
- Output Held more than Half Clock Cycle
- One Clock Operation
- 0.9W Power Dissipation
- Single Power Supply

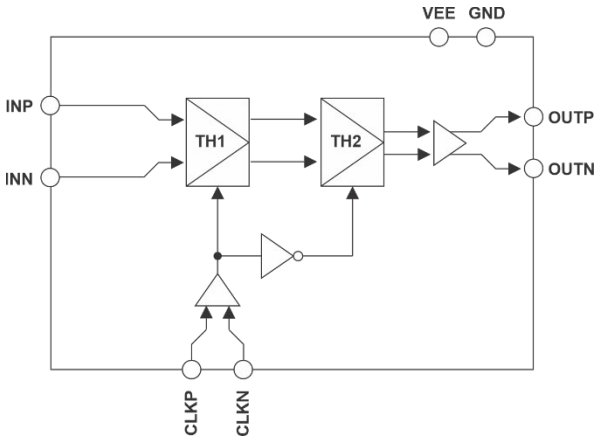

Figure 1 - Functional Block Diagram.

Product Description

RTH122's bandwidth and aperture jitter enable 1 to 4 GS/s accurate sampling of DC to multi-GHz signals. The differential-to-differential dual track-and-hold cascades two track-and-hold circuits, TH1 and TH2. The RTH122 provides a held output for more than half a clock cycle, easing bandwidth requirements of subsequent circuitry relative to the case of a single track-and-hold (TH). The RTH122 works with a single clock simplifying clock distribution.

Ordering information

PART NUMBER	DESCRIPTION
RTH122-HQ	24 Pin QFP Package
RTH122-HB	24 Pin QFP Package – Class B
RTH122-QN	20 IO QFN Package
RTH122-DI	Die
EVRTH122	Evaluation Module

CAUTION
DEVICE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)

Absolute Maximum Ratings

Supply Voltages

VEE to GND ……..……..…..... -6 V

Input Voltages

INP, INN to GND …..……..……..……+10 dBm
CLKP, CLKN to GND ……..…...-2.7±1.0 V

Temperature

Junction Temperature ……..….. +150 °C
Operating Board Temperature ……..….. +105 °C
Lead, Soldering (10 Seconds) …….. +220 °C
Storage Temperature..…… -65 to +150 °C

ESD

HBM model (Class 0B) ……..…….. >125 V

DC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.4V; Clock: 4GHz, 0.6Vpp Differential; Input: 300mV Single-Ended.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
1.0	**DC TRANSFER FUNCTION**						
1.1	Gain	G	Over Entire Bandwidth	-1		3	dB
2.0	**TEMPERATURE DRIFT**						
2.1	Warm-up Time		After Power-up		0		s
3.0	**ANALOG INPUT (INP, INN)**						
3.1	Common Mode Voltage	IN_{CM}			0		mV
3.2	Input Impedance	R_{IIN}	Each Lead to GND		50		Ω
4.0	**CLOCK INPUT (CLKP, CLKN)**						
4.1	Input Resistance	R_{CIN}	Differential		100		Ω
5.0	**ANALOG OUTPUT (OUTP, OUTN)**						
5.1	Output Resistance	R_{OUT}	Each Output to GND		50		Ω
5.2	Maximum Current		Into Output Lead			20	mA
5.3	Output Common Mode	V_{OCM}	Outputs Terminated with 50 Ohm to GND		-0.5		V
5.4	Output Offset Voltage	V_{OFF}	Absolute Value (No Input Signal)		20	40	mV
6.0	**POWER SUPPLY REQUIREMENTS**						
6.1	Negative Supply Current	IEE			170	220	mA
6.2	Power Dissipation	P			0.9	1.2	W

AC Electrical Specification – CLK = 1GHz

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.4V; Clock: 1GHz, 0.6Vpp Differential.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
7.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.1Vpp SINGLE ENDED**						
7.1	Bandwidth	BW	-3dB Gain, 0.1 V_{PP} Single Ended Input		26		GHz
7.2	SFDR						
	50 MHz	SFDR	0.1 Vpp Single Ended Input		60		dBc
	2050 MHz	SFDR	0.1 Vpp Single Ended Input		60		dBc
	4050 MHz	SFDR	0.1 Vpp Single Ended Input		56		dBc
	6050 MHz	SFDR	0.1 Vpp Single Ended Input		55		dBc
	8050 MHz	SFDR	0.1 Vpp Single Ended Input		44		dBc
	10050 MHz	SFDR	0.1 Vpp Single Ended Input		37		dBc
	12050 MHz	SFDR	0.1 Vpp Single Ended Input		35		dBc
	14050 MHz	SFDR	0.1 Vpp Single Ended Input		39		dBc
	16050 MHz	SFDR	0.1 Vpp Single Ended Input		47		dBc
	18050 MHz	SFDR	0.1 Vpp Single Ended Input		32		dBc
	20050 MHz	SFDR	0.1 Vpp Single Ended Input		30		dBc
	21050 MHz	SFDR	0.1 Vpp Single Ended Input		37		dBc
	22050 MHz	SFDR	0.1 Vpp Single Ended Input		44		dBc
	23050 MHz	SFDR	0.1 Vpp Single Ended Input		38		dBc
	24050 MHz	SFDR	0.1 Vpp Single Ended Input		36		dBc
	25050 MHz	SFDR	0.1 Vpp Single Ended Input		36		dBc
	26050 MHz	SFDR	0.1 Vpp Single Ended Input		36		dBc
	27050 MHz	SFDR	0.1 Vpp Single Ended Input		37		dBc
	28050 MHz	SFDR	0.1 Vpp Single Ended Input		37		dBc
7.3	THD						
	50 MHz	THD	0.1 Vpp Single Ended Input		-55		dBc
	2050 MHz	THD	0.1 Vpp Single Ended Input		-54		dBc
	4050 MHz	THD	0.1 Vpp Single Ended Input		-52		dBc
	6050 MHz	THD	0.1 Vpp Single Ended Input		-52		dBc
	8050 MHz	THD	0.1 Vpp Single Ended Input		-44		dBc
	10050 MHz	THD	0.1 Vpp Single Ended Input		-37		dBc
	12050 MHz	THD	0.1 Vpp Single Ended Input		-35		dBc
	14050 MHz	THD	0.1 Vpp Single Ended Input		-39		dBc
	16050 MHz	THD	0.1 Vpp Single Ended Input		-46		dBc
	18050 MHz	THD	0.1 Vpp Single Ended Input		-32		dBc
	20050 MHz	THD	0.1 Vpp Single Ended Input		-30		dBc
	21050 MHz	THD	0.1 Vpp Single Ended Input		-37		dBc
	22050 MHz	THD	0.1 Vpp Single Ended Input		-43		dBc
	23050 MHz	THD	0.1 Vpp Single Ended Input		-37		dBc
	24050 MHz	THD	0.1 Vpp Single Ended Input		-36		dBc
	25050 MHz	THD	0.1 Vpp Single Ended Input		-36		dBc
	26050 MHz	THD	0.1 Vpp Single Ended Input		-38		dBc
	27050 MHz	THD	0.1 Vpp Single Ended Input		-37		dBc
	28050 MHz	THD	0.1 Vpp Single Ended Input		-37		dBc

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
8.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.3Vpp SINGLE ENDED**						
8.1	Bandwidth	BW	-3dB Gain, 0.3 V_{PP} Single Ended Input		25		GHz
8.2	SFDR						
	50 MHz	SFDR	0.3 Vpp Single Ended Input		63		dBc
	2050 MHz	SFDR	0.3 Vpp Single Ended Input		62		dBc
	4050 MHz	SFDR	0.3 Vpp Single Ended Input		47		dBc
	6050 MHz	SFDR	0.3 Vpp Single Ended Input		47		dBc
	8050 MHz	SFDR	0.3 Vpp Single Ended Input		35		dBc
	10050 MHz	SFDR	0.3 Vpp Single Ended Input		27		dBc
	12050 MHz	SFDR	0.3 Vpp Single Ended Input		25		dBc
	14050 MHz	SFDR	0.3 Vpp Single Ended Input		29		dBc
	16050 MHz	SFDR	0.3 Vpp Single Ended Input		38		dBc
	18050 MHz	SFDR	0.3 Vpp Single Ended Input		23		dBc
	20050 MHz	SFDR	0.3 Vpp Single Ended Input		21		dBc
	21050 MHz	SFDR	0.3 Vpp Single Ended Input		27		dBc
	22050 MHz	SFDR	0.3 Vpp Single Ended Input		34		dBc
	23050 MHz	SFDR	0.3 Vpp Single Ended Input		28		dBc
	24050 MHz	SFDR	0.3 Vpp Single Ended Input		27		dBc
	25050 MHz	SFDR	0.3 Vpp Single Ended Input		27		dBc
	26050 MHz	SFDR	0.3 Vpp Single Ended Input		27		dBc
	27050 MHz	SFDR	0.3 Vpp Single Ended Input		28		dBc
	28050 MHz	SFDR	0.3 Vpp Single Ended Input		28		dBc
8.3	THD						
	50 MHz	THD	0.3 Vpp Single Ended Input		-61		dBc
	2050 MHz	THD	0.3 Vpp Single Ended Input		-60		dBc
	4050 MHz	THD	0.3 Vpp Single Ended Input		-47		dBc
	6050 MHz	THD	0.3 Vpp Single Ended Input		-47		dBc
	8050 MHz	THD	0.3 Vpp Single Ended Input		-35		dBc
	10050 MHz	THD	0.3 Vpp Single Ended Input		-27		dBc
	12050 MHz	THD	0.3 Vpp Single Ended Input		-25		dBc
	14050 MHz	THD	0.3 Vpp Single Ended Input		-29		dBc
	16050 MHz	THD	0.3 Vpp Single Ended Input		-38		dBc
	18050 MHz	THD	0.3 Vpp Single Ended Input		-23		dBc
	20050 MHz	THD	0.3 Vpp Single Ended Input		-21		dBc
	21050 MHz	THD	0.3 Vpp Single Ended Input		-27		dBc
	22050 MHz	THD	0.3 Vpp Single Ended Input		-34		dBc
	23050 MHz	THD	0.3 Vpp Single Ended Input		-28		dBc
	24050 MHz	THD	0.3 Vpp Single Ended Input		-27		dBc
	25050 MHz	THD	0.3 Vpp Single Ended Input		-27		dBc
	26050 MHz	THD	0.3 Vpp Single Ended Input		-27		dBc
	27050 MHz	THD	0.3 Vpp Single Ended Input		-28		dBc
	28050 MHz	THD	0.3 Vpp Single Ended Input		-28		dBc

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
9.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.5Vpp SINGLE ENDED**						
9.1	Bandwidth	BW	-3dB Gain, 0.5 V_{PP} Single Ended Input		24		GHz
9.2	SFDR						
	50 MHz	SFDR	0.5 Vpp Single Ended Input		58		dBc
	2050 MHz	SFDR	0.5 Vpp Single Ended Input		58		dBc
	4050 MHz	SFDR	0.5 Vpp Single Ended Input		43		dBc
	6050 MHz	SFDR	0.5 Vpp Single Ended Input		43		dBc
	8050 MHz	SFDR	0.5 Vpp Single Ended Input		31		dBc
	10050 MHz	SFDR	0.5 Vpp Single Ended Input		23		dBc
	12050 MHz	SFDR	0.5 Vpp Single Ended Input		21		dBc
	14050 MHz	SFDR	0.5 Vpp Single Ended Input		25		dBc
	16050 MHz	SFDR	0.5 Vpp Single Ended Input		33		dBc
	18050 MHz	SFDR	0.5 Vpp Single Ended Input		18		dBc
	20050 MHz	SFDR	0.5 Vpp Single Ended Input		17		dBc
	21050 MHz	SFDR	0.5 Vpp Single Ended Input		23		dBc
	22050 MHz	SFDR	0.5 Vpp Single Ended Input		30		dBc
	23050 MHz	SFDR	0.5 Vpp Single Ended Input		24		dBc
	24050 MHz	SFDR	0.5 Vpp Single Ended Input		23		dBc
	25050 MHz	SFDR	0.5 Vpp Single Ended Input		24		dBc
	26050 MHz	SFDR	0.5 Vpp Single Ended Input		24		dBc
	27050 MHz	SFDR	0.5 Vpp Single Ended Input		25		dBc
	28050 MHz	SFDR	0.5 Vpp Single Ended Input		25		dBc
9.3	THD						
	50 MHz	THD	0.5 Vpp Single Ended Input		-55		dBc
	2050 MHz	THD	0.5 Vpp Single Ended Input		-56		dBc
	4050 MHz	THD	0.5 Vpp Single Ended Input		-43		dBc
	6050 MHz	THD	0.5 Vpp Single Ended Input		-42		dBc
	8050 MHz	THD	0.5 Vpp Single Ended Input		-30		dBc
	10050 MHz	THD	0.5 Vpp Single Ended Input		-23		dBc
	12050 MHz	THD	0.5 Vpp Single Ended Input		-21		dBc
	14050 MHz	THD	0.5 Vpp Single Ended Input		-25		dBc
	16050 MHz	THD	0.5 Vpp Single Ended Input		-33		dBc
	18050 MHz	THD	0.5 Vpp Single Ended Input		-18		dBc
	20050 MHz	THD	0.5 Vpp Single Ended Input		-17		dBc
	21050 MHz	THD	0.5 Vpp Single Ended Input		-23		dBc
	22050 MHz	THD	0.5 Vpp Single Ended Input		-30		dBc
	23050 MHz	THD	0.5 Vpp Single Ended Input		-24		dBc
	24050 MHz	THD	0.5 Vpp Single Ended Input		-23		dBc
	25050 MHz	THD	0.5 Vpp Single Ended Input		-24		dBc
	26050 MHz	THD	0.5 Vpp Single Ended Input		-24		dBc
	27050 MHz	THD	0.5 Vpp Single Ended Input		-25		dBc
	28050 MHz	THD	0.5 Vpp Single Ended Input		-25		dBc

AC Electrical Specification – CLK = 2GHz

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.4V; Clock: 2GHz, 0.6Vpp Differential;

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
10.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.1Vpp SINGLE ENDED**						
10.1	Bandwidth	BW	-3dB Gain, 0.1 V_{PP} Single Ended Input		26		GHz
10.2	SFDR						
	50 MHz	SFDR	0.1 Vpp Single Ended Input		61		dBc
	2050 MHz	SFDR	0.1 Vpp Single Ended Input		57		dBc
	4050 MHz	SFDR	0.1 Vpp Single Ended Input		60		dBc
	6050 MHz	SFDR	0.1 Vpp Single Ended Input		59		dBc
	8050 MHz	SFDR	0.1 Vpp Single Ended Input		55		dBc
	10050 MHz	SFDR	0.1 Vpp Single Ended Input		47		dBc
	12050 MHz	SFDR	0.1 Vpp Single Ended Input		42		dBc
	14050 MHz	SFDR	0.1 Vpp Single Ended Input		45		dBc
	16050 MHz	SFDR	0.1 Vpp Single Ended Input		47		dBc
	18050 MHz	SFDR	0.1 Vpp Single Ended Input		39		dBc
	20050 MHz	SFDR	0.1 Vpp Single Ended Input		36		dBc
	22050 MHz	SFDR	0.1 Vpp Single Ended Input		48		dBc
	24050 MHz	SFDR	0.1 Vpp Single Ended Input		42		dBc
	26050 MHz	SFDR	0.1 Vpp Single Ended Input		41		dBc
	28050 MHz	SFDR	0.1 Vpp Single Ended Input		41		dBc
10.3	THD						
	50 MHz	THD	0.1 Vpp Single Ended Input		-57		dBc
	2050 MHz	THD	0.1 Vpp Single Ended Input		-57		dBc
	4050 MHz	THD	0.1 Vpp Single Ended Input		-56		dBc
	6050 MHz	THD	0.1 Vpp Single Ended Input		-55		dBc
	8050 MHz	THD	0.1 Vpp Single Ended Input		-53		dBc
	10050 MHz	THD	0.1 Vpp Single Ended Input		-46		dBc
	12050 MHz	THD	0.1 Vpp Single Ended Input		-42		dBc
	14050 MHz	THD	0.1 Vpp Single Ended Input		-45		dBc
	16050 MHz	THD	0.1 Vpp Single Ended Input		-47		dBc
	18050 MHz	THD	0.1 Vpp Single Ended Input		-39		dBc
	20050 MHz	THD	0.1 Vpp Single Ended Input		-36		dBc
	22050 MHz	THD	0.1 Vpp Single Ended Input		-47		dBc
	24050 MHz	THD	0.1 Vpp Single Ended Input		-42		dBc
	26050 MHz	THD	0.1 Vpp Single Ended Input		-41		dBc
	28050 MHz	THD	0.1 Vpp Single Ended Input		-40		dBc

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
11.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.3Vpp SINGLE ENDED**						
11.1	Bandwidth	BW	-3dB Gain, 0.3 V_{PP} Single Ended Input		26		GHz
11.2	SFDR						
	50 MHz	SFDR	0.3 Vpp Single Ended Input		64		dBc
	2050 MHz	SFDR	0.3 Vpp Single Ended Input		60		dBc
	4050 MHz	SFDR	0.3 Vpp Single Ended Input		57		dBc
	6050 MHz	SFDR	0.3 Vpp Single Ended Input		54		dBc
	8050 MHz	SFDR	0.3 Vpp Single Ended Input		46		dBc
	10050 MHz	SFDR	0.3 Vpp Single Ended Input		37		dBc
	12050 MHz	SFDR	0.3 Vpp Single Ended Input		32		dBc
	14050 MHz	SFDR	0.3 Vpp Single Ended Input		36		dBc
	16050 MHz	SFDR	0.3 Vpp Single Ended Input		38		dBc
	18050 MHz	SFDR	0.3 Vpp Single Ended Input		29		dBc
	20050 MHz	SFDR	0.3 Vpp Single Ended Input		27		dBc
	22050 MHz	SFDR	0.3 Vpp Single Ended Input		39		dBc
	24050 MHz	SFDR	0.3 Vpp Single Ended Input		32		dBc
	26050 MHz	SFDR	0.3 Vpp Single Ended Input		31		dBc
	28050 MHz	SFDR	0.3 Vpp Single Ended Input		31		dBc
11.3	THD						
	50 MHz	THD	0.3 Vpp Single Ended Input		-61		dBc
	2050 MHz	THD	0.3 Vpp Single Ended Input		-59		dBc
	4050 MHz	THD	0.3 Vpp Single Ended Input		-56		dBc
	6050 MHz	THD	0.3 Vpp Single Ended Input		-52		dBc
	8050 MHz	THD	0.3 Vpp Single Ended Input		-45		dBc
	10050 MHz	THD	0.3 Vpp Single Ended Input		-37		dBc
	12050 MHz	THD	0.3 Vpp Single Ended Input		-32		dBc
	14050 MHz	THD	0.3 Vpp Single Ended Input		-36		dBc
	16050 MHz	THD	0.3 Vpp Single Ended Input		-38		dBc
	18050 MHz	THD	0.3 Vpp Single Ended Input		-29		dBc
	20050 MHz	THD	0.3 Vpp Single Ended Input		-27		dBc
	22050 MHz	THD	0.3 Vpp Single Ended Input		-38		dBc
	24050 MHz	THD	0.3 Vpp Single Ended Input		-32		dBc
	26050 MHz	THD	0.3 Vpp Single Ended Input		-31		dBc
	28050 MHz	THD	0.3 Vpp Single Ended Input		-31		dBc

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
12.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.5Vpp SINGLE ENDED**						
12.1	Bandwidth	BW	-3dB Gain, 0.5 V_{PP} Single Ended Input		25		GHz
12.2	SFDR						
	50 MHz	SFDR	0.5 Vpp Single Ended Input		58		dBc
	2050 MHz	SFDR	0.5 Vpp Single Ended Input		56		dBc
	4050 MHz	SFDR	0.5 Vpp Single Ended Input		52		dBc
	6050 MHz	SFDR	0.5 Vpp Single Ended Input		47		dBc
	8050 MHz	SFDR	0.5 Vpp Single Ended Input		41		dBc
	10050 MHz	SFDR	0.5 Vpp Single Ended Input		33		dBc
	12050 MHz	SFDR	0.5 Vpp Single Ended Input		29		dBc
	14050 MHz	SFDR	0.5 Vpp Single Ended Input		32		dBc
	16050 MHz	SFDR	0.5 Vpp Single Ended Input		33		dBc
	18050 MHz	SFDR	0.5 Vpp Single Ended Input		25		dBc
	20050 MHz	SFDR	0.5 Vpp Single Ended Input		22		dBc
	22050 MHz	SFDR	0.5 Vpp Single Ended Input		34		dBc
	24050 MHz	SFDR	0.5 Vpp Single Ended Input		29		dBc
	26050 MHz	SFDR	0.5 Vpp Single Ended Input		28		dBc
	28050 MHz	SFDR	0.5 Vpp Single Ended Input		29		dBc
12.3	THD						
	50 MHz	THD	0.5 Vpp Single Ended Input		-56		dBc
	2050 MHz	THD	0.5 Vpp Single Ended Input		-54		dBc
	4050 MHz	THD	0.5 Vpp Single Ended Input		-51		dBc
	6050 MHz	THD	0.5 Vpp Single Ended Input		-45		dBc
	8050 MHz	THD	0.5 Vpp Single Ended Input		-39		dBc
	10050 MHz	THD	0.5 Vpp Single Ended Input		-32		dBc
	12050 MHz	THD	0.5 Vpp Single Ended Input		-28		dBc
	14050 MHz	THD	0.5 Vpp Single Ended Input		-32		dBc
	16050 MHz	THD	0.5 Vpp Single Ended Input		-33		dBc
	18050 MHz	THD	0.5 Vpp Single Ended Input		-25		dBc
	20050 MHz	THD	0.5 Vpp Single Ended Input		-22		dBc
	22050 MHz	THD	0.5 Vpp Single Ended Input		-34		dBc
	24050 MHz	THD	0.5 Vpp Single Ended Input		-28		dBc
	26050 MHz	THD	0.5 Vpp Single Ended Input		-28		dBc
	28050 MHz	THD	0.5 Vpp Single Ended Input		-29		dBc

AC Electrical Specification – CLK = 4GHz

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.4V; Clock: 4GHz, 0.6Vpp Differential;

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
13.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.1Vpp SINGLE ENDED**						
13.1	Bandwidth	BW	-3dB Gain, 0.1 V_{PP} Single Ended Input		25		GHz
13.2	SFDR						
	50 MHz	SFDR	0.1 Vpp Single Ended Input		63		dBc
	4050 MHz	SFDR	0.1 Vpp Single Ended Input		61		dBc
	8050 MHz	SFDR	0.1 Vpp Single Ended Input		56		dBc
	12050 MHz	SFDR	0.1 Vpp Single Ended Input		45		dBc
	16050 MHz	SFDR	0.1 Vpp Single Ended Input		47		dBc
	20050 MHz	SFDR	0.1 Vpp Single Ended Input		41		dBc
	24050 MHz	SFDR	0.1 Vpp Single Ended Input		47		dBc
	28050 MHz	SFDR	0.1 Vpp Single Ended Input		45		dBc
13.3	THD						
	50 MHz	THD	0.1 Vpp Single Ended Input		-59		dBc
	4050 MHz	THD	0.1 Vpp Single Ended Input		-58		dBc
	8050 MHz	THD	0.1 Vpp Single Ended Input		-54		dBc
	12050 MHz	THD	0.1 Vpp Single Ended Input		-45		dBc
	16050 MHz	THD	0.1 Vpp Single Ended Input		-47		dBc
	20050 MHz	THD	0.1 Vpp Single Ended Input		-41		dBc
	24050 MHz	THD	0.1 Vpp Single Ended Input		-47		dBc
	28050 MHz	THD	0.1 Vpp Single Ended Input		-45		dBc
14.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.3Vpp SINGLE ENDED**						
14.1	Bandwidth	BW	-3dB Gain, 0.3 V_{PP} Single Ended Input		25		GHz
14.2	SFDR						
	50 MHz	SFDR	0.3 Vpp Single Ended Input		62		dBc
	4050 MHz	SFDR	0.3 Vpp Single Ended Input		53		dBc
	8050 MHz	SFDR	0.3 Vpp Single Ended Input		47		dBc
	12050 MHz	SFDR	0.3 Vpp Single Ended Input		35		dBc
	16050 MHz	SFDR	0.3 Vpp Single Ended Input		38		dBc
	20050 MHz	SFDR	0.3 Vpp Single Ended Input		31		dBc
	24050 MHz	SFDR	0.3 Vpp Single Ended Input		37		dBc
	28050 MHz	SFDR	0.3 Vpp Single Ended Input		36		dBc
14.3	THD						
	50 MHz	THD	0.3 Vpp Single Ended Input		-61		dBc
	4050 MHz	THD	0.3 Vpp Single Ended Input		-52		dBc
	8050 MHz	THD	0.3 Vpp Single Ended Input		-46		dBc
	12050 MHz	THD	0.3 Vpp Single Ended Input		-35		dBc
	16050 MHz	THD	0.3 Vpp Single Ended Input		-38		dBc
	20050 MHz	THD	0.3 Vpp Single Ended Input		-31		dBc
	24050 MHz	THD	0.3 Vpp Single Ended Input		-37		dBc
	28050 MHz	THD	0.3 Vpp Single Ended Input		-36		dBc

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
15.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.5Vpp SINGLE ENDED**						
15.1	Bandwidth	BW	-3dB Gain, 0.5 V_{PP} Single Ended Input		24		GHz
15.2	SFDR						
	50 MHz	SFDR	0.5 Vpp Single Ended Input		58		dBc
	4050 MHz	SFDR	0.5 Vpp Single Ended Input		48		dBc
	8050 MHz	SFDR	0.5 Vpp Single Ended Input		41		dBc
	12050 MHz	SFDR	0.5 Vpp Single Ended Input		31		dBc
	16050 MHz	SFDR	0.5 Vpp Single Ended Input		33		dBc
	20050 MHz	SFDR	0.5 Vpp Single Ended Input		27		dBc
	24050 MHz	SFDR	0.5 Vpp Single Ended Input		34		dBc
	28050 MHz	SFDR	0.5 Vpp Single Ended Input		33		dBc
15.3	THD						
	50 MHz	THD	0.5 Vpp Single Ended Input		-56		dBc
	4050 MHz	THD	0.5 Vpp Single Ended Input		-48		dBc
	8050 MHz	THD	0.5 Vpp Single Ended Input		-40		dBc
	12050 MHz	THD	0.5 Vpp Single Ended Input		-31		dBc
	16050 MHz	THD	0.5 Vpp Single Ended Input		-33		dBc
	20050 MHz	THD	0.5 Vpp Single Ended Input		-27		dBc
	24050 MHz	THD	0.5 Vpp Single Ended Input		-33		dBc
	28050 MHz	THD	0.5 Vpp Single Ended Input		-33		dBc

AC Electrical Specification

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
16.0	**TRACK TO HOLD SWITCHING AND HOLD STATE, TH1**						
16.1	Aperture Delay	ta	After V(CLKP) – V(CLKN) Goes Neg. *		-25		ps
16.2	Settling Time to 1 mV	ts	At Hold Capacitors. Ttrack1,min Observed *		60		ps
16.3	Diff. Droop Rate/V_{IN}		Initial Droop Rate *		5		%/ns
16.4	Aperture Jitter	taj	Fclk = 4GHz *			60	fs
17.0	**AC TRANSFER FUNCTION**						
17.1	Gain	G_{BW}	Gain over total bandwidth	-2.25	0	4	dB

* NOTE: Values from simulation.

Return Loss

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
18.0	**INPUT RETURN LOSS**						
18.1	DC – 5GHz	In Return Loss	0.3Vpp Single Ended 25MHz Step Size	10			dB
18.2	5GHz - 15GHz	In Return Loss	0.3Vpp Single Ended 25MHz Step Size	5			dB
18.3	15GHz – 20GHz	Int Return Loss	0.3Vpp Single Ended 25MHz Step Size	4			dB
19.0	**OUTPUT RETURN LOSS**						
19.1	DC – 1.5GHz	Out Return Loss	0.3Vpp Single Ended 25MHz Step Size	18			dB
19.2	1.5GHz – 3GHz	Out Return Loss	0.3Vpp Single Ended 25MHz Step Size	15			dB
19.3	3GHz – 5GHz	Out Return Loss	0.3Vpp Single Ended 25MHz Step Size	10			dB

Operating Conditions

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
20.0	**CLOCK INPUT (CLKP, CLKN)**						
20.1	Amplitude	V_{CPP}	Differential	450	600	1000	mVpp
20.2	Common Mode Voltage	V_{CCM}			-2.7		V
20.3	CLK Frequency	F_{CLK}		1000		4000	MHz
21.0	**ANALOG INPUT (INP, INN)**						
21.1	Full Scale Range	FSR	Differential			1000	mVpp
21.2	Common Mode Voltage	V_{CM}	When DC Coupled		0		mV
22.0	**ANALOG OUTPUT (OUTP, OUTN)**						
22.1	Ext. Termination Voltage	V_{TERM}	See Fig 5 for Output Termination		0		V
22.2	Ext. Termination Resistor	R_{TERM}	Required From Outputs To Vterm		50		Ω
23.0	**POWER SUPPLY REQUIREMENTS**						
23.1	Negative Supply Voltage	VEE		-5.2	-5.4	-5.6	V
24.0	**OPERATING TEMPERATURE**[1]						
24.1	Case Temperature	Tc		-40		85	°C

[1] The part is designed to maintain high performance operation within a case temperature range of -40 ~ 85°C and we recommend not to exceed the Absolute Maximum Temperature shown on page 2. For the best performance, operation within the specified temperature range with proper heat dissipation is recommended. The metal pad where the part is soldered should be connected to the ground plane with thermal vias for better heat dissipation. A heatsink can be attached to the bottom of the PCB, on a metal pad connected to the metal pad where the part is soldered.

Pin Description and Pin Out (24 Lead QFP Package)

P/I/O	PIN	NUM.	NAME	FUNCTION
P	1,2,4,6,7,10,11,12,13, 14,16,18,19,20,22,24, bottom plate	17	GND	Power Supply Ground
P	21, 23	2	VEE	Negative Power Supply
I	8	1	CLKP	Clock Input: High = TH1 in Track Mode Low = TH1 in Hold Mode
I	9	1	CLKN	
I	3	1	INP	Analog Input
I	5	1	INN	
O	17	1	OUTP	Analog Output
O	15	1	OUTN	

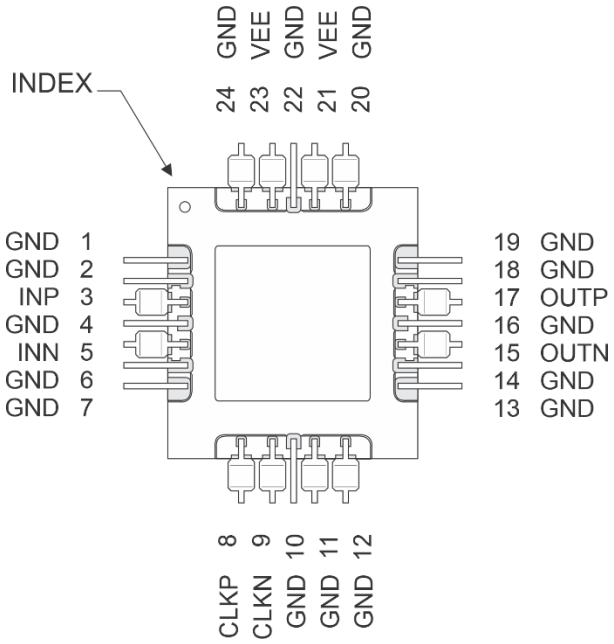

Figure 2 – RTH122 pinout (top view) 24 lead QFP package.

Pin Description and Pin Out (20 IO QFN Package)

P/I/O	PIN	NUM.	NAME	FUNCTION
P	1,3,5,8,9,10,11,13,15, 16,18,20,bottom plate	13	GND	Power Supply Ground
P	17, 19	2	VEE	Negative Power Supply
I	6	1	CLKP	Clock Input: High = TH1 in Track Mode
I	7	1	CLKN	Low = TH1 in Hold Mode
I	2	1	INP	Analog Input
I	4	1	INN	
O	14	1	OUTP	Analog Output
O	12	1	OUTN	

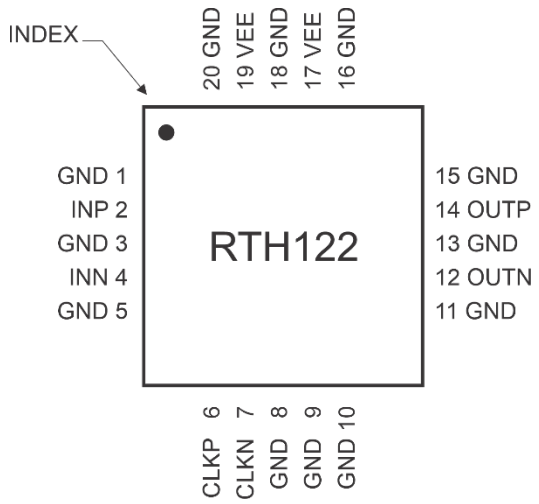

Figure 3 – RTH122 pinout (top view) 20 IO QFN package.

Definitions of Terms

Acquisition Time (tacq). The delay between the time a track-and-hold circuit (TH) enters track mode and the time the TH hold capacitor nodes track the input within some specified precision. The acquisition time sets a lower limit on the required track time during clocked operation.

Aperture Delay (ta). The average (or mean value) of the delay between the hold command (input clock switched from track to hold state) and the instant at which the analog input is sampled. The time is positive if the clock path delay is longer than the signal path delay. It is negative if the signal path delay is longer than the clock path delay.

Aperture Jitter (Δt). The standard deviation of the delay between the hold command (input clock switched from track-to-hold state) and the instant at which the analog input is sampled, excluding clock source jitter. It is the total jitter if the clock source is jitter free (ideal). Jitter diverges slowly as measurement time increases because of "1/f" noise, important at low frequencies (< 10 kHz). The specified jitter takes into account the white noise sources only (thermal and shot noise). For high-speed samplers this is reasonable, since even long data records span a time shorter than the time scale important for 1/f noise. For white-noise caused jitter, the clock and aperture jitter can be added in an rms manner to obtain the total sampling jitter.

Clock Jitter. The standard deviation of the mid-points of the relevant (rising or falling) edge of the clock source relative to the ideal edge (best fit). This jitter can be derived from the phase noise of the clock source, where the lower frequency bound of integration should correspond to the duration of a measurement record that the source will be used for.

Common-Mode Rejection Ratio (CMRR). Proportionality coefficient of the differential output and the common mode component of input signal. If an ideal symmetric input is available, CMR is the ratio of the differential output to the input on either input pin. A high-quality 50-ohm splitter may be used to generate the symmetrical inputs.

Full Scale Range (FSR). The maximum difference between the highest and lowest input levels for which various device performance specifications hold, unless otherwise noted.

Gain. Ratio of output signal magnitude to input signal magnitude. For sinewave inputs, it is the ratio of the amplitude of the first (main) harmonic output (HD1) to the amplitude of the input.

Input Bandwidth (BW). The input frequency at which the gain for sinewave input is reduced by 3 dB relative to its value at low frequencies. The low frequency range is defined as the range including DC over which the gain stays essentially constant. The high frequency range is characterized by an increase in gain variation versus frequency, at least including the eventual monotonic decrease of the gain ("roll-off"). The input bandwidth tends to be input amplitude dependent. It is normally largest for very small inputs and smallest for FSR inputs.

Settling Time (ts). The delay between the time that a track-and-hold circuit (TH) enters hold mode and the time that the TH hold capacitor nodes settle to within some specified precision. The settling time sets a lower limit on the required hold time during clocked operation.

Spurious Free Dynamic Range (SFDR). The ratio of the magnitude of the first (main) harmonic, HD1, and the highest other harmonic (or non-harmonic other tone, if present), as observed in the TH spectrum. The input is FSR, unless otherwise noted. SFDR in dB is given by 20log (SFDR as amplitude ratio), and is generally positive.

Total Harmonic Distortion (THD). The ratio of the square root of the sum of the harmonics 2 to 5 to the amplitude of the first (main) harmonic in the TH spectrum. THD in dB is given by 20log (THD as amplitude ratio), and is generally negative.

Theory of Operation

The RTH122 chip contains two TH's, TH1 and TH2, in series, together with clock shaping circuitry, and a 50-ohm output driver (Figure 1). To maximize dynamic range and insensitivity to noise, all non-DC internal circuits and all non-DC inputs and outputs are differential. TH1 determines the dynamic sampled-mode performance of the track and hold. TH1 clock inputs (CLKTH1) are derived directly from CLKP and CLKN and should be driven by a low-jitter clock source. TH2 is similar to TH1, except that its bandwidth requirement is lower.

The track and hold receive a differential analog input signal at inputs INP and INN, which is sampled on the TH1 hold capacitors upon a falling transition of its differential clock voltage V(CLKTH1P) – V(CLKTH1N), after an aperture delay, ta, see Figure 3. TH1's aperture delay is negative, nominally 25ps.

The sampling instant is affected by clock source jitter (off-chip) and aperture jitter (caused by on-chip noise).

The held and buffered output of TH1, VTH1, is sampled on the TH2 hold capacitors upon a falling transition of its differential clock voltage V(CLKTH2P) – V(CLKTH2N), after an aperture delay of TH1. This allows simple out-of-phase clocking of TH1 and TH2 by having opposite phases for CLKTH1 and CLKTH2. Aperture jitter of TH2 is irrelevant, since the slew rate of the TH2 input is equal to the TH1 differential droop rate. TH2 can be in track mode before TH1 switches to hold, but a minimum track time of TH2 after TH1 enters hold mode must be observed to ensure that TH2 has fully acquired the TH1 output.

Lower limits for the sampling rates of TH1 and TH2 are set by single-ended hold-mode droop rates, and lead to the specification of maximum hold times. For longer hold times, the RTH122 must be allowed sufficient recovery time during track phase (or a sequence of track phases), so it can return to normal operation mode.

Signal Descriptions

The RTH122 inputs are terminated on-chip with 50 Ω to GND. This automatically protects against off-chip high-impedance high-voltage disturbances. The absolute maximum rated voltage at input termination resistors is 1 V. The RTH122 is designed for 1 Vpp differential input signals. If operated in single-ended mode, the complementary input is self biased and can be left unconnected. Distortion in the single-ended mode will be higher than in differential mode, and differential input should be used for optimal performance. The INP and INN inputs are equivalent, except for the polarity of their effect on OUTP and OUTN.

The differential clock input signal (P and N) is terminated on-chip with 50 Ω to GND. Use differential clock signal for optimal performance. Large CLK edge rate benefits aperture jitter performance, small CLK amplitudes minimizes distortion due to clock feed-through in the higher clock frequency range. The RTH122 can also operate using single ended clock. Distortion for single-ended clock can be several dB higher than for differential clock, and differential clock should be used for optimal performance.

Due to its highly differential design, the RTH122 requires relatively modest power supply decoupling. The smaller decoupling capacitors from VEE to GND should be placed as close to the package as possible. Larger low frequency power supply decoupling capacitors, VEE to GND, should be placed within 1 inch of the RTH122. Depending on the expected noise on the supplies more capacitors in parallel may need to be used. With low-impedance supplies that are very quiet (no digital circuitry), the RTH122 can also perform well with no external decoupling at all.

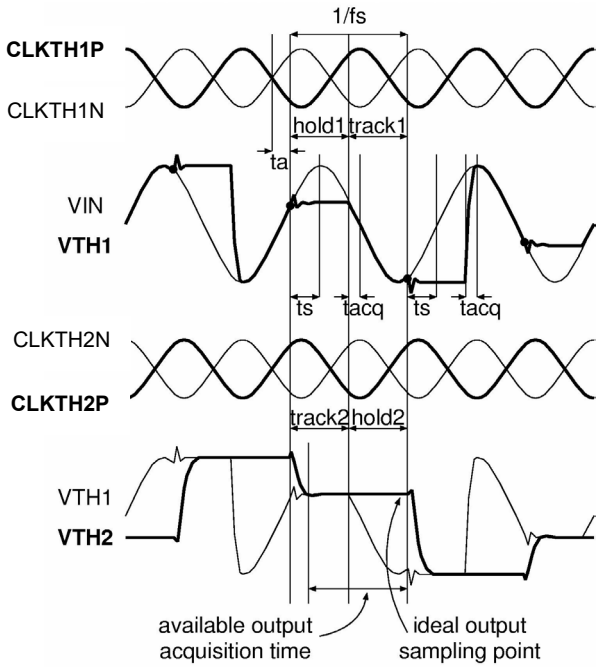

Figure 4 - Timing diagram for out-of-phase clocking of TH1 and TH2.

Typical Operating Circuit

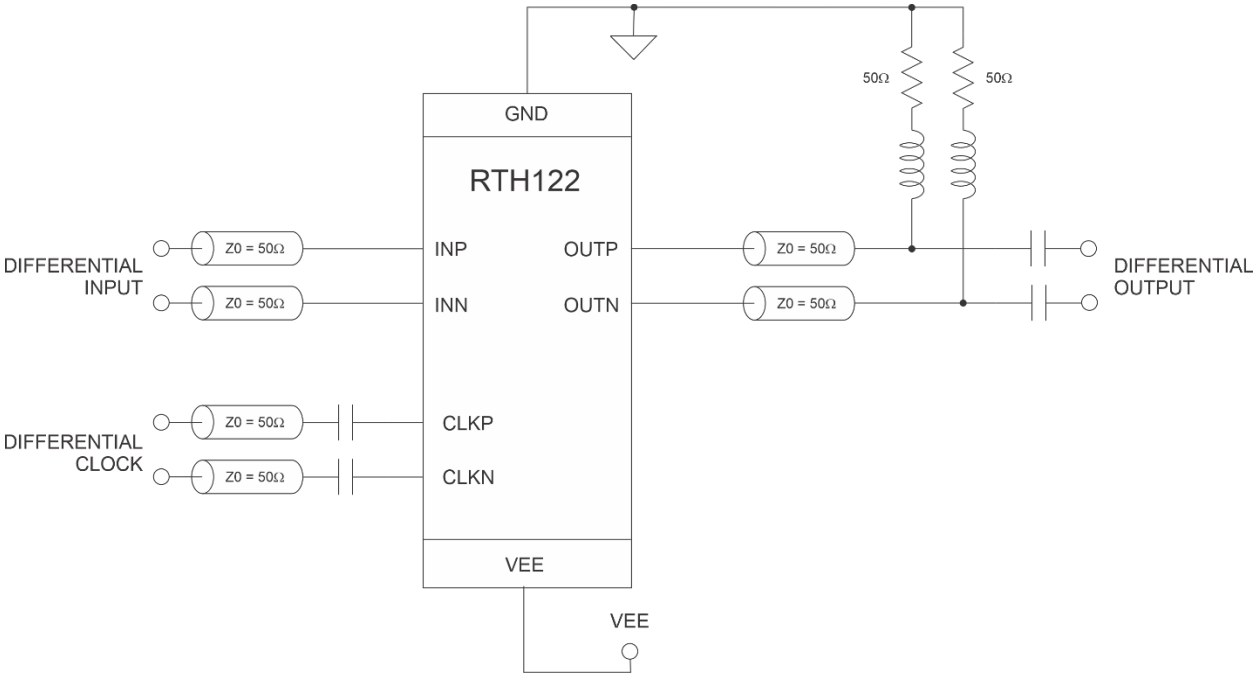

Figure 5- Typical interface circuit.

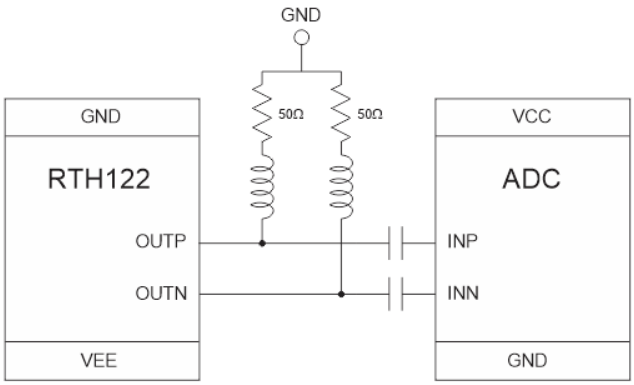

Figure 6 - Typical interface circuit to an ADC with internal 50 Ohm termination to AC Ground.

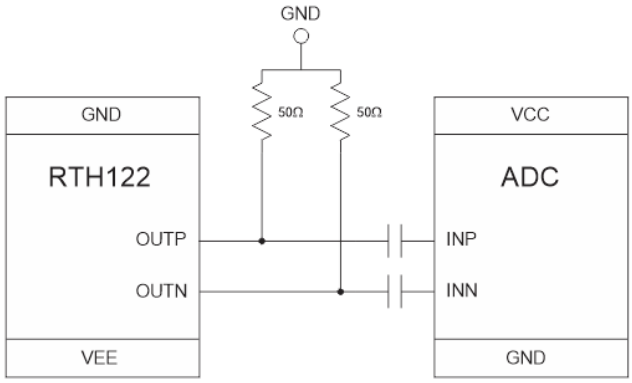

Figure 7 - Typical interface circuit to an ADC with high impedance inputs.

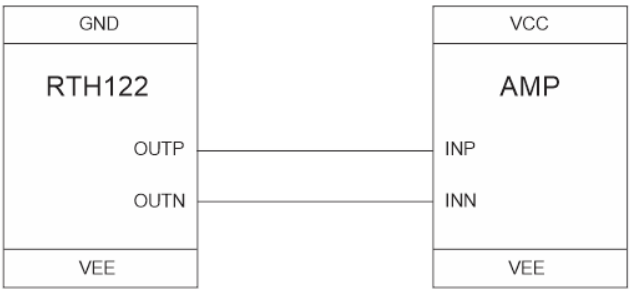

Figure 8 – It is possible to direct connect the RTH122 to an Amplifier or other circuits as long as they comply with the RTH122 output common mode and are able to supply the necessary DC current.

Equivalent Circuit

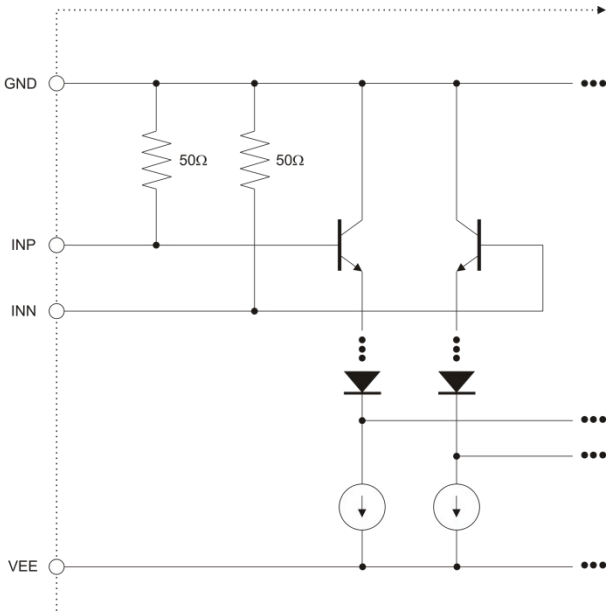

Figure 9 – Input RF equivalent circuit.

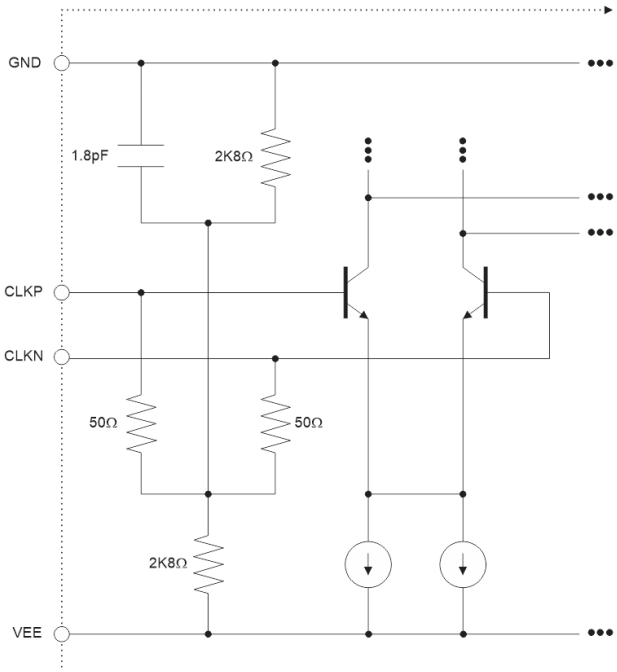

Figure 10 – Clock equivalent circuit.

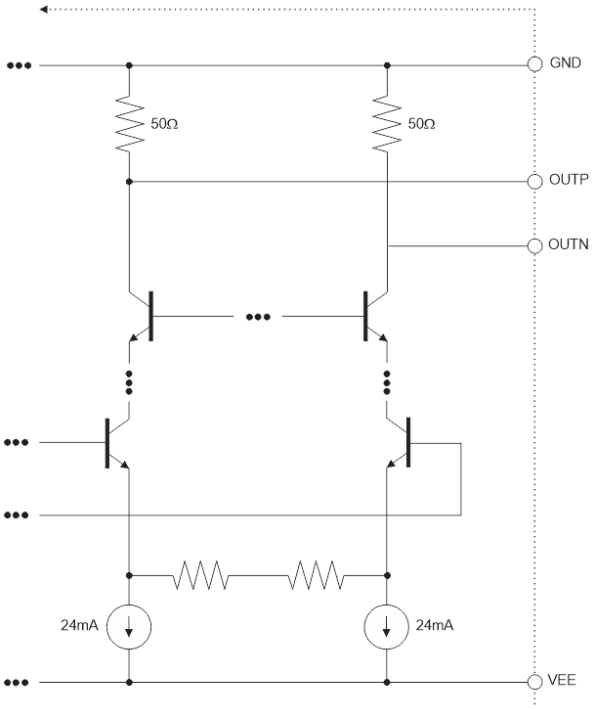

Figure 11 – Output equivalent circuit.

Typical Performance 1GHz Clock

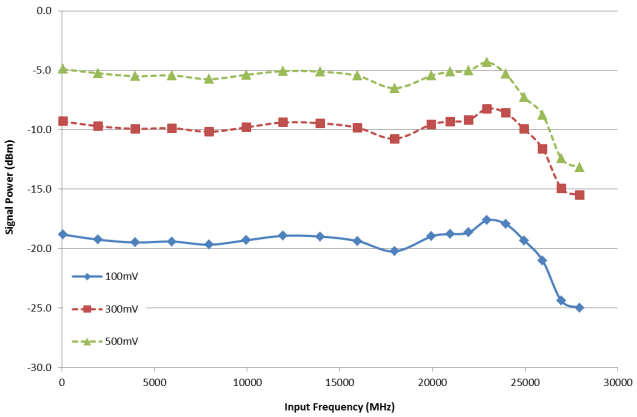

Figure 12 - Input Bandwidth, single ended input.

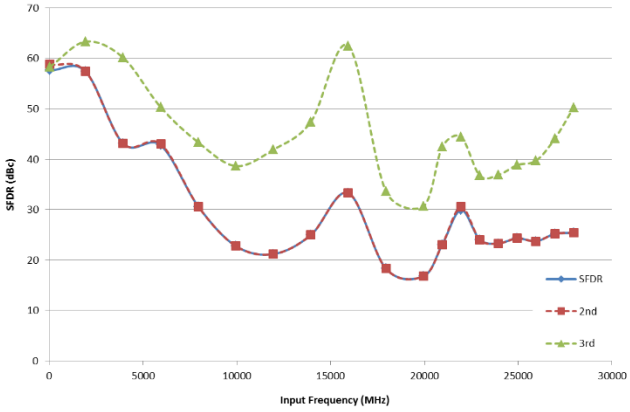

Figure 13 - SFDR, 500mVpp input, single ended.

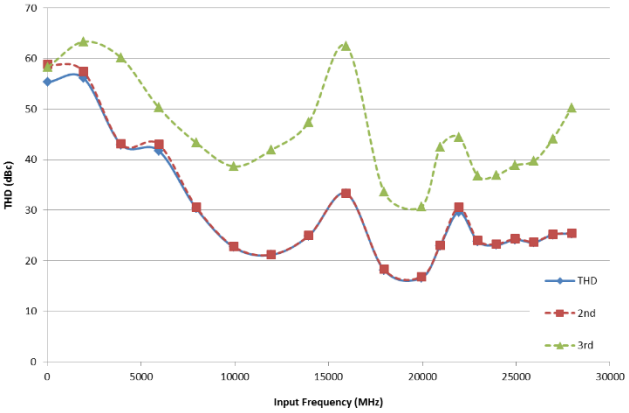

Figure 14 - THD, 500mVpp input, single ended.

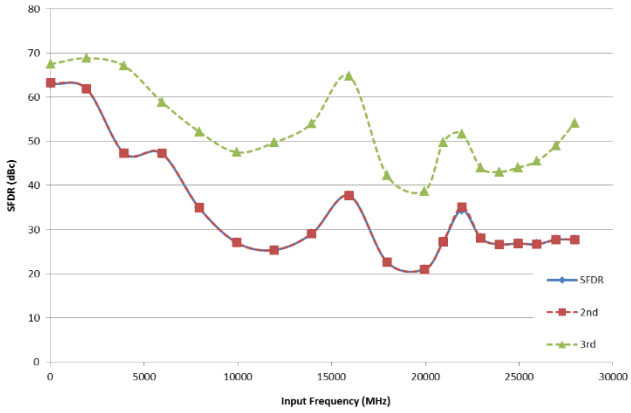

Figure 15 - SFDR, 300mVpp input, single ended.

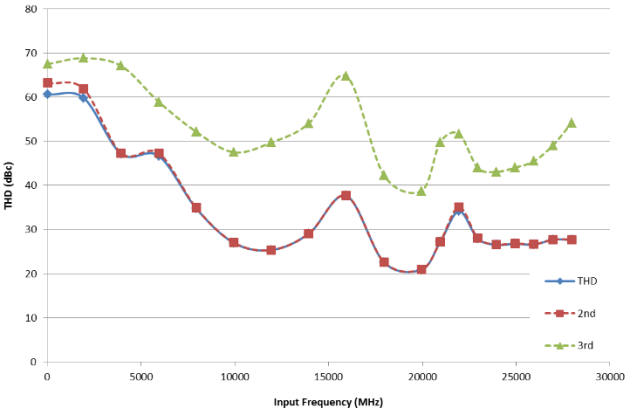

Figure 16 – THD, 300mVpp input, single ended.

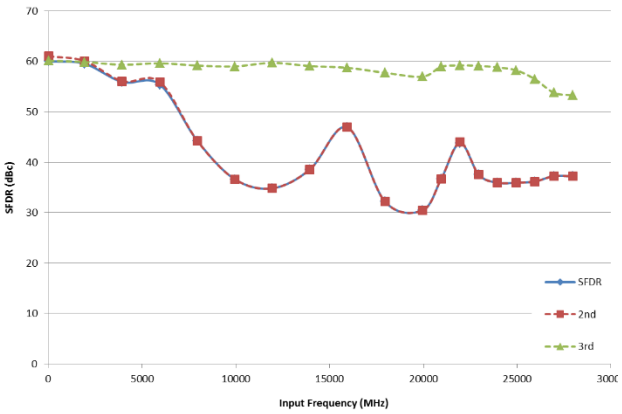

Figure 17 - SFDR, 100mVpp input, single ended.

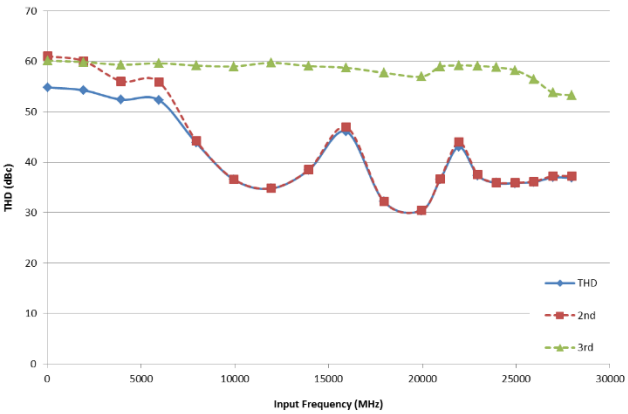

Figure 18 - THD, 100mVpp input, single ended.

Typical Performance 2GHz Clock

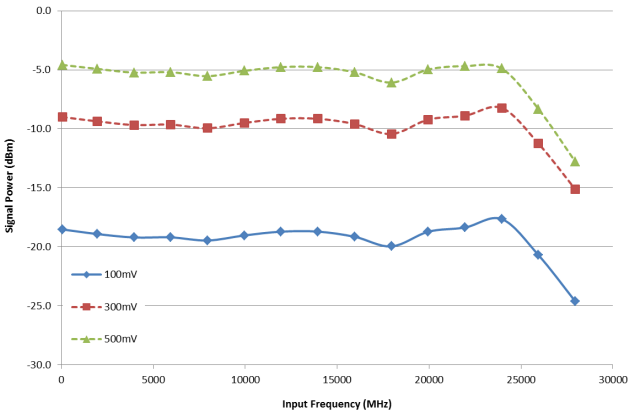

Figure 19 - Input Bandwidth, single ended input.

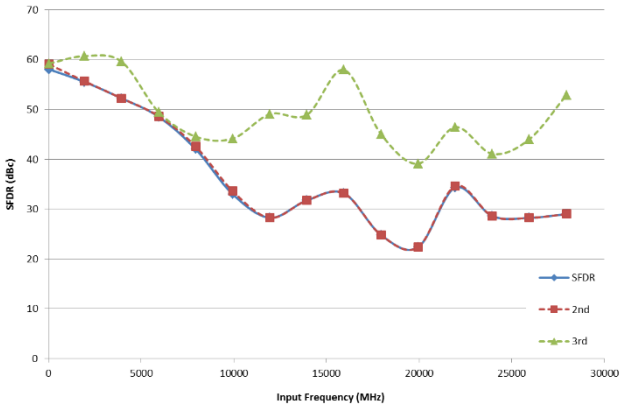

Figure 20 - SFDR, 500mVpp input, single ended.

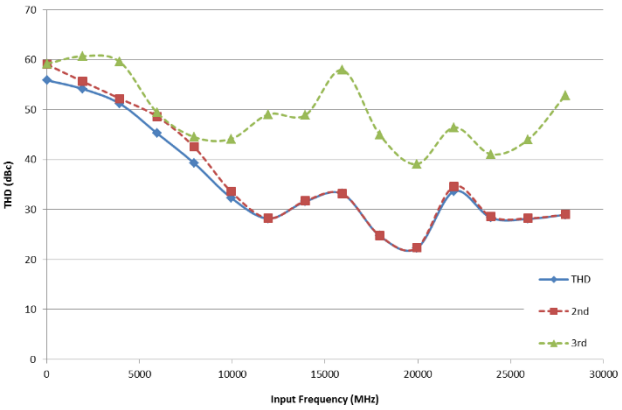

Figure 21 - THD, 500mVpp input, single ended.

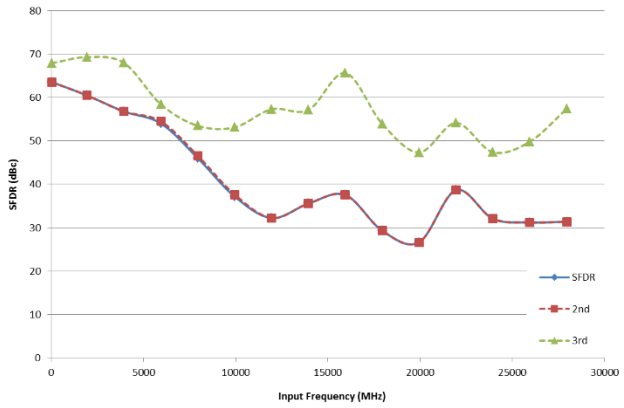

Figure 22 - SFDR, 300mVpp input, single ended.

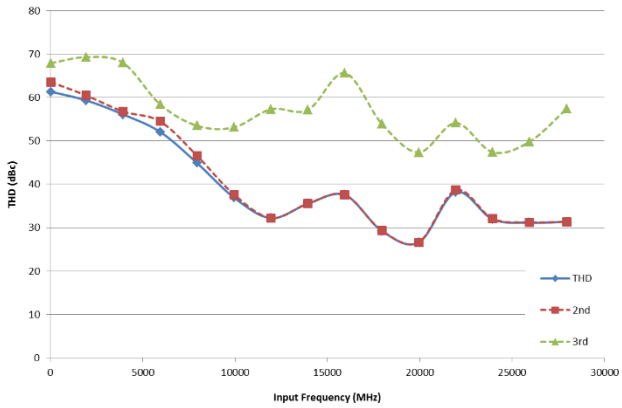

Figure 23 – THD, 300mVpp input, single ended.

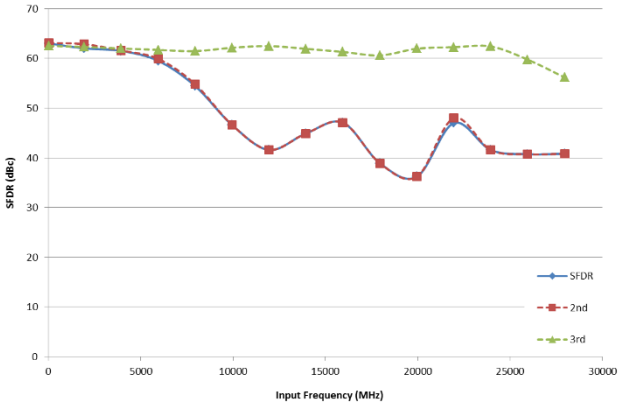

Figure 24 - SFDR, 100mVpp input, single ended.

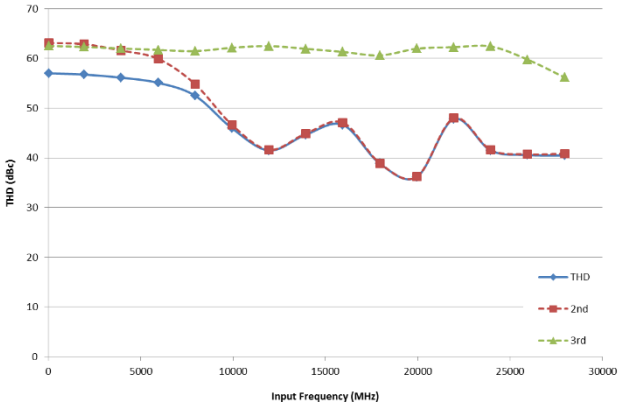

Figure 25 - THD, 100mVpp input, single ended.

Typical Performance 4GHz Clock

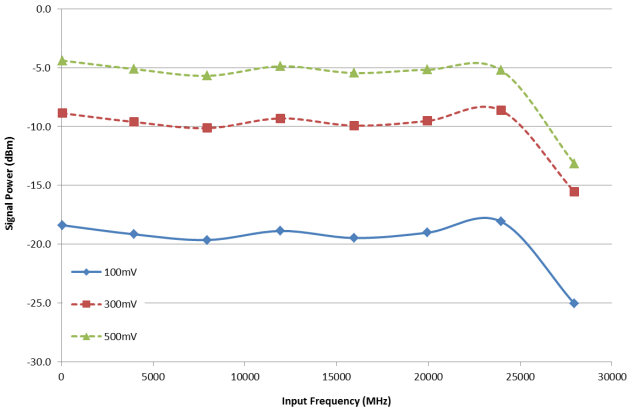

Figure 26 - Input Bandwidth, single ended input.

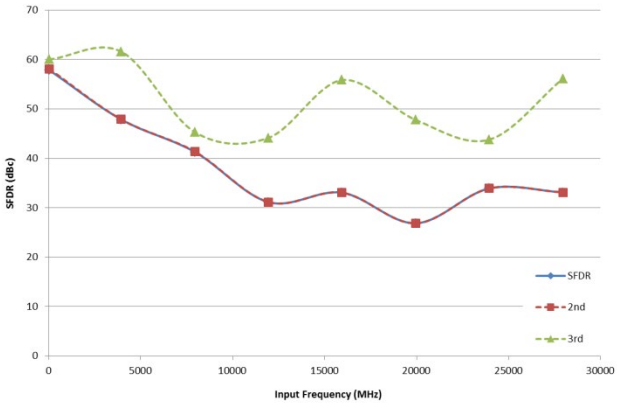

Figure 27 - SFDR, 500mVpp input, single ended.

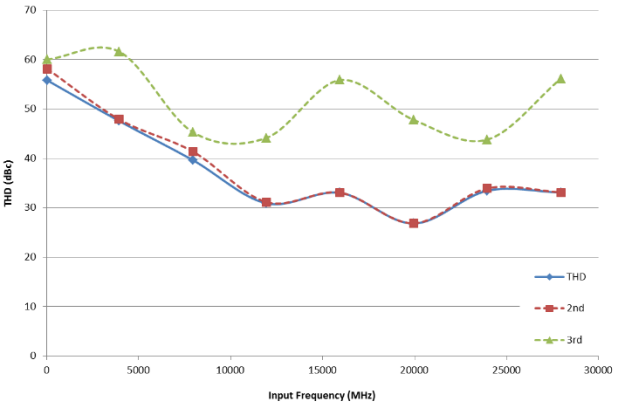

Figure 28 - THD, 500mVpp input, single ended.

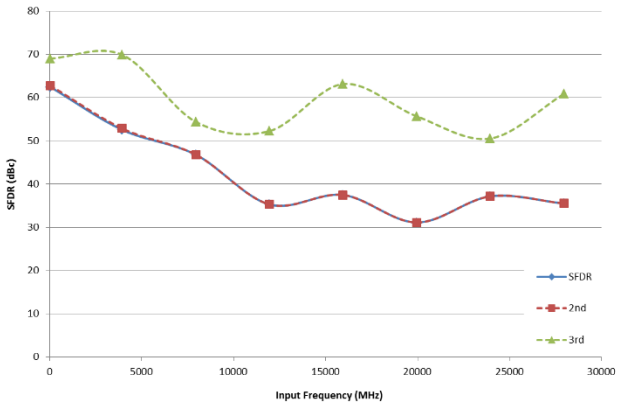

Figure 29 - SFDR, 300mVpp input, single ended.

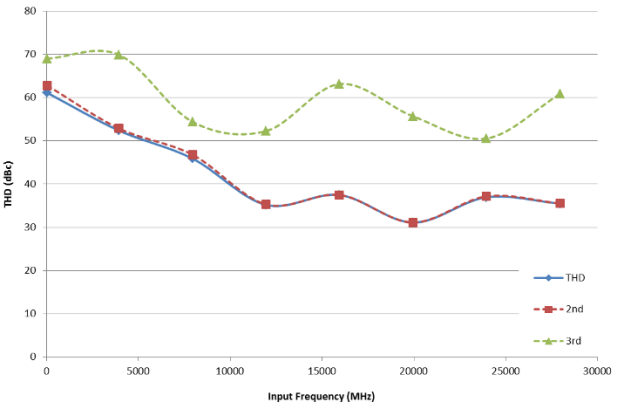

Figure 30 – THD, 300mVpp input, single ended.

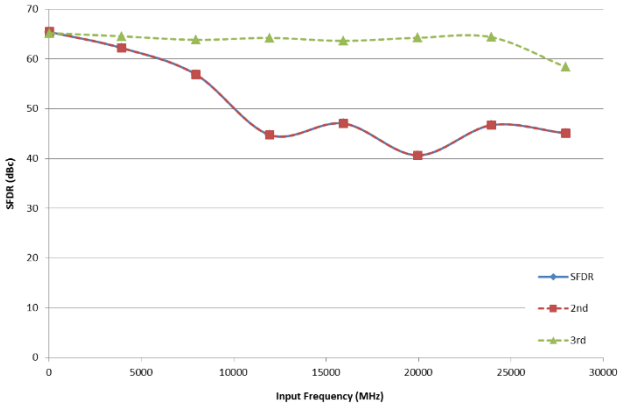

Figure 31 - SFDR, 100mVpp input, single ended.

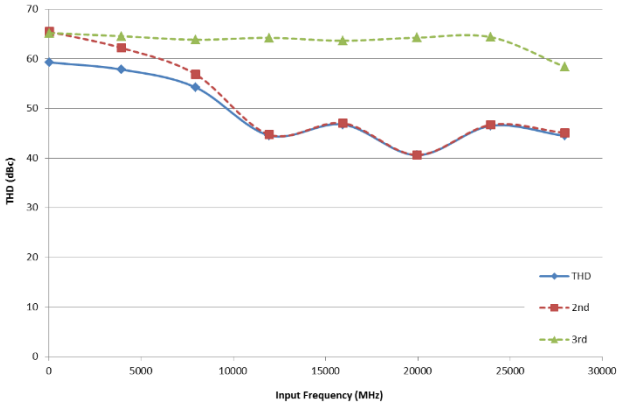

Figure 32 - THD, 100mVpp input, single ended.

Package Information -HQ, -HB

The package is a high-speed 24 lead QFP with a Cu/Mo metal pad at the bottom.

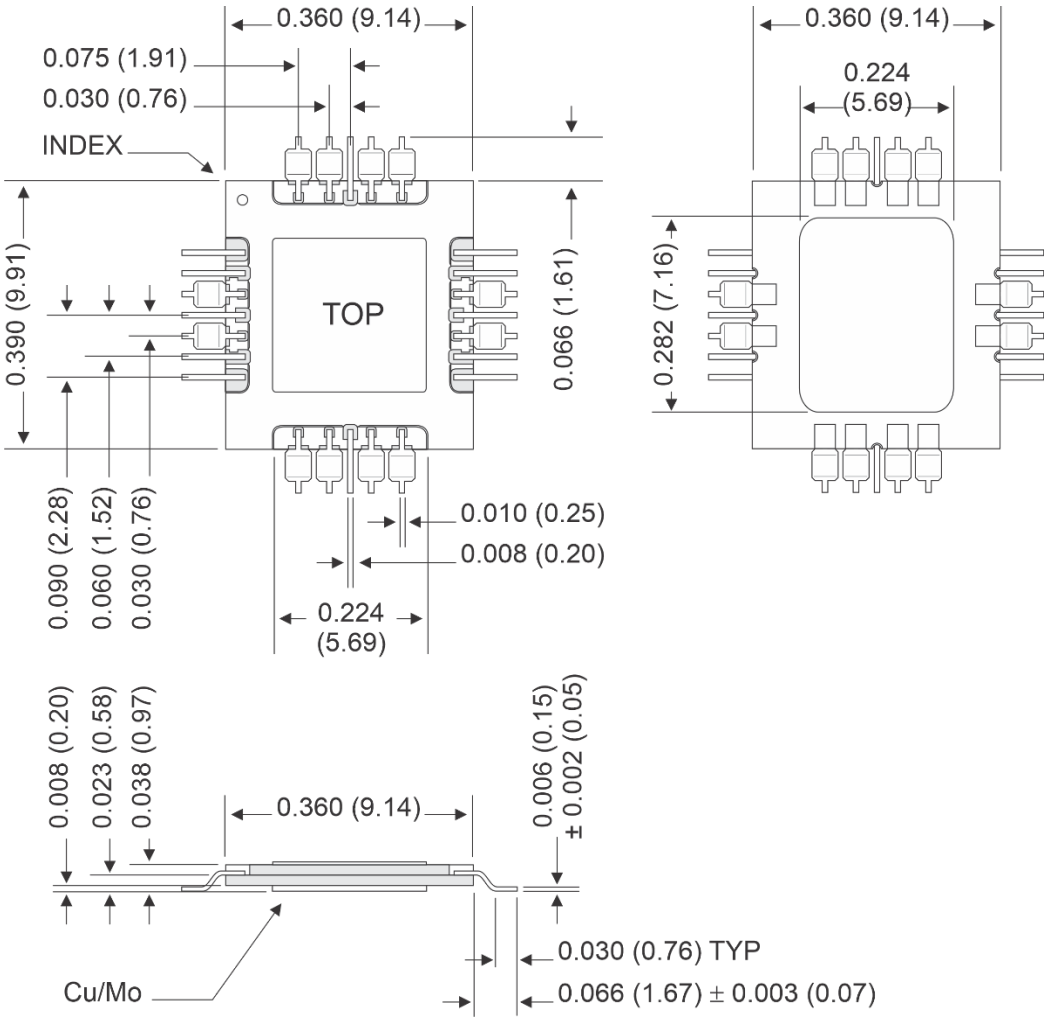

Figure 33 – RTH122-HQ (-HB) package outline, dimensions in inches (mm).

Package Information -QN

The package is a 20 IO QFN. The metal pad at the bottom is electrical ground and should be used for heat dissipation.

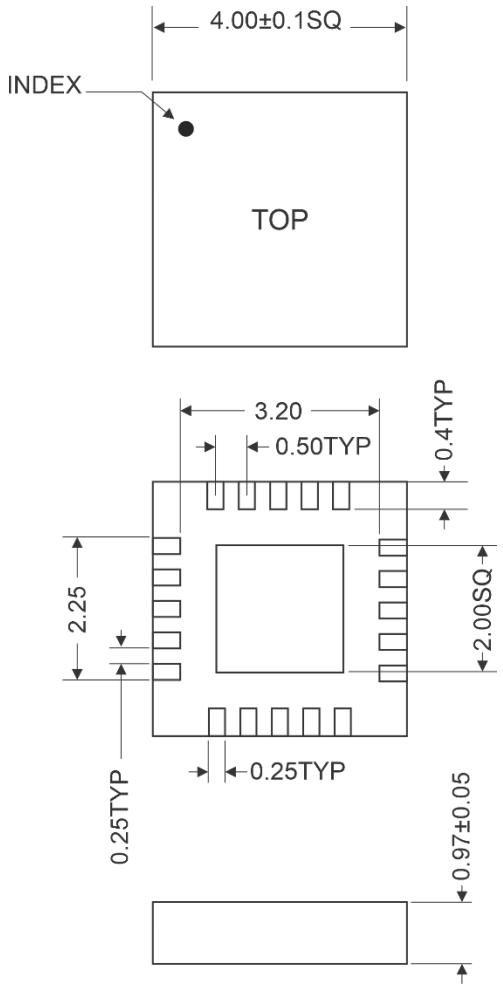

Figure 34 – RTH122-QN package outline, dimensions in mm.