TELEDYNE SCIENTIFIC COMPANY

EVRDA112M4MSLPD

12 Bit 2.0 GS/s Low Power Master-Slave Differential 4:1 MUXDAC Evaluation Board

Features

- Single ended SMA data input
- Open Input Option: Samtec edge connector interface
- Fully Assembled and Tested DAC for your evaluation and prototyping needs

Product Description

The EVRDA112M4MSLPD-BG is an evaluation board designed to demonstrate the performance of the RDA112M4MSLPD-BG, a 2.0GS/s digital-to-analog converter. The evaluation kit is composed of three boards: The SMA connector board with all the data and low clock connections; the buffer board that convert the single ended data input signals to differential signals; and the DUT board which hold the DAC and its controls. The boards are fully assembled and tested, providing an easy way to evaluate the DAC performance.

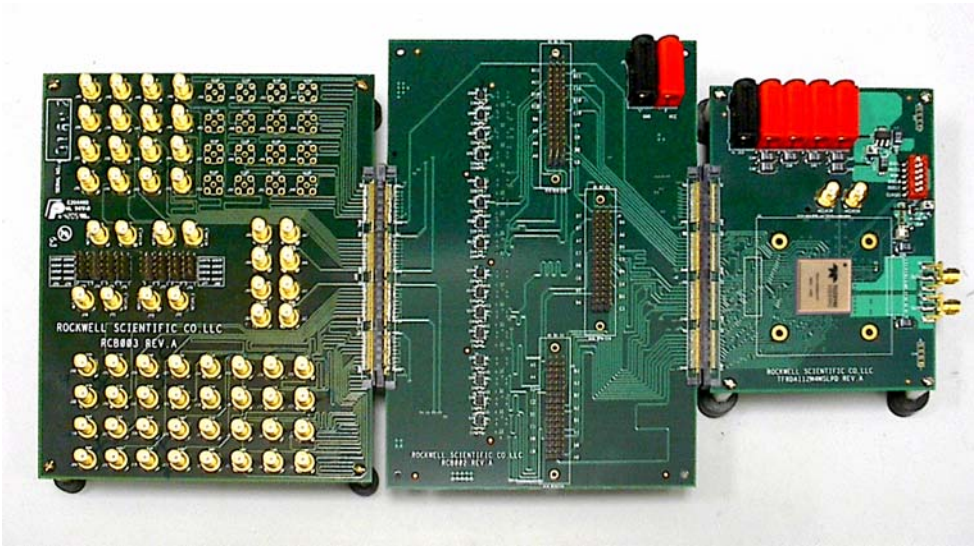

Figure 1 – EVRDA112M4MSLPD-BG

Ordering information

PART NUMBER	DESCRIPTION
EVRDA112M4MSLPD-BG	RDA112M4MSLPD-BG Evaluation Board

Signal Description

Power Supplies

The evaluation board requires separate positive 2.5V and 3.3V supplies and the buffer board requires a 3.3V supply. Connect the power supplies to the boards using banana cables. There is no need for power-up sequencing.

VDDIO - I/O circuit supply (2.5V)
VDD33 – Digital supply (3.3V)
VDD25 – Digital supply (2.5V)
VDDA – Analog supply (3.3V)

Inputs

The data can be supplied to the RDA112M4MSLPD by using the SMA connectors in the connector board or directly to the DUT board using the Samtec high-speed connector. The signals are single ended in the SMA connector board ($V_{IL,MAX}$=-400mV, $V_{IH,MIN}$=400mV) and differential when using the Samtec connector (LVDS compatible). When using the Samtec high-speed connector please refer to the board schematic for details. Please note that the data assignment in the Samtec connector in the DUT board differs from the specification contained in the RBUS2 datasheet. The connections for channels A & B are routed on the topside of the board and C & D are routed on the bottom while in the RBUS2 the channels A & C are on top. The difference between the two implementations is a swap between channels B and C.

The high frequency clock (operating clock HCLK) needs to come from a DC blocked source with LVPECL compatible amplitude.

When using the SMA connector board the LCLKI and the LCLKO are accessible through CLKA and CLKB respectively. They are LVDS compatible.

VREF is a +1.3V reference that is derived from the power supplies and made available to the RDA112M4MSLPD. Potentiometer R5 in this circuit may have to be adjusted to achieve the nominal +1.3V. A test point is provided for probing purposes. It is a good idea to check that VREF is nominally +1.3V after power up to achieve optimum performance from the RDA112M4MSLPD. Likewise, potentiometer R4 may need adjustment to ensure a VTT value of +2V, the termination voltage for the differential sampling clock.

Outputs

The analog output (OUTP, OUTN) of the RDA112M4MSLPD is available on the SMA connectors J5 & J6. The outputs need a DC path to 3.3V that can be provided with a 50Ohm termination to 3.3V or when using measuring equipment that already have a 50Ohm termination to GND by using a bias-T connected to 3.3V with its choke on the DAC output side.

PC Board Layout

The EVRDA112M4MSLPD is fabricated using six layers of Hi Tg FR4 material. The thickness of the board is 62 +/- 7 mils.

All data and clock signals are treated as 50Ω transmission lines. Figure 2 is the layer stack of the evaluation board, including layer thickness.

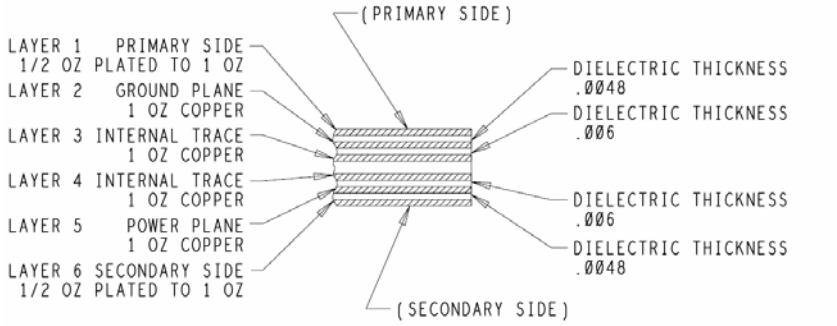

Figure 2 – EVRDA112M4MSLPD layer stack

Components

Table 1: Jumper and Test Point List

DESIGNATOR / SIGNAL	SETTINGS	FUNCTION
S1 / BSEL, MXSEL, MSM, DSEL0, DSEL1, CLKSEL	BSEL : Always OFF	Control Selection Switch
	MXSEL OFF: 4:1 Mode ON: 2:1 Mode	
	MSM OFF: MASTER ON: SLAVE	
	DSEL <0:1> OFF,OFF: 1 HCLK Delay ON,OFF: 2 HCLK Delay OFF,ON: 3 HCLK Delay ON,ON: 4 HCLK Delay	
	CLKSEL OFF: DDR Mode ON: SDR Mode	
J4 / VREF*	1-2 OPEN: Internal VREF 1-2 CLOSED: External VREF	VREF Selection
J7 / VTT	Nominally +2V	VTT Test Point
J8 / VREF	Between +1.2 and +1.6V	VREF Test Point
J14 / GND		GND Points
J15 / GND		GND Points

* In this version J4 is hardwired to CLOSED

Table 2: Component List

DESIGNATOR	QTY	DESCRIPTION
C2-C20, C42-C46	23	15pF C0402C150J5GAC-TU (0402 size)
C1	1	1nF C0402C103J3RAC
C21-C41, C44	22	10uF Capacitors (293D106X9016C2T)
R4	1	100Ω Potentiometer (3223W-1-101E)
R5	1	20KΩ Potentiometer (3223W-1-203E)
R3	1	50 Ω Resistor (0603 size)
R3, R4	2	50Ω Resistor (0805 size)
R2, R6	2	1KΩ Resistor (0603 size)
R7	1	250Ω Resistor (0603 size)
S1	1	Dip Switch (SDA06H1SKD)
J4, J14, J15	1	4x1 Header
U1	1	RDA112M4MSLPD-BG
J1	1	Edge Connector (QSE-080-01-F-D-EM2)
J5, J6	2	SMA Edge Connector (142-0701-851)
J9-J13	4	Banana Plug Sockets
J2, J3	2	SMA Connector (142-0701-201)
U2	1	Adjustable Regulator (LT1117)
U3	1	Shunt Regulator (TLV431ASNT1)

Board Configuration

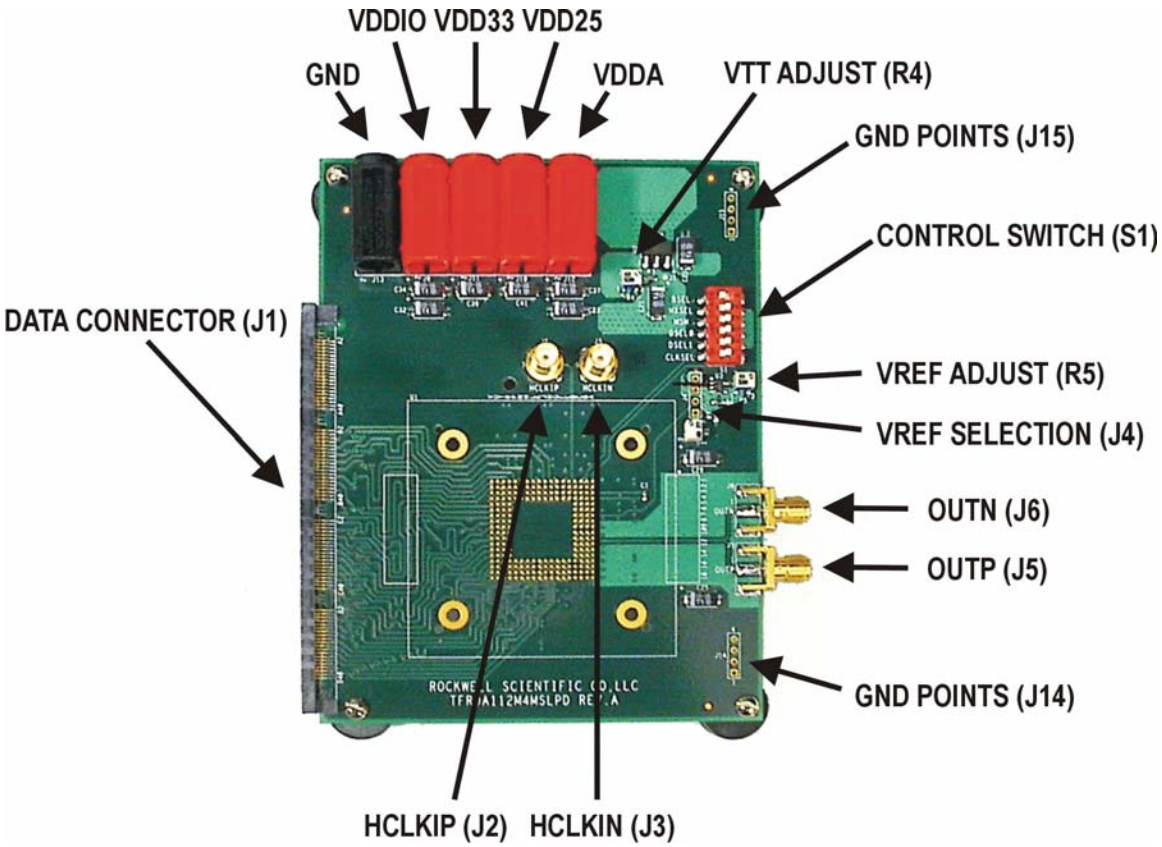

Figure 3 – EVRDA112M4MSLPD board configuration

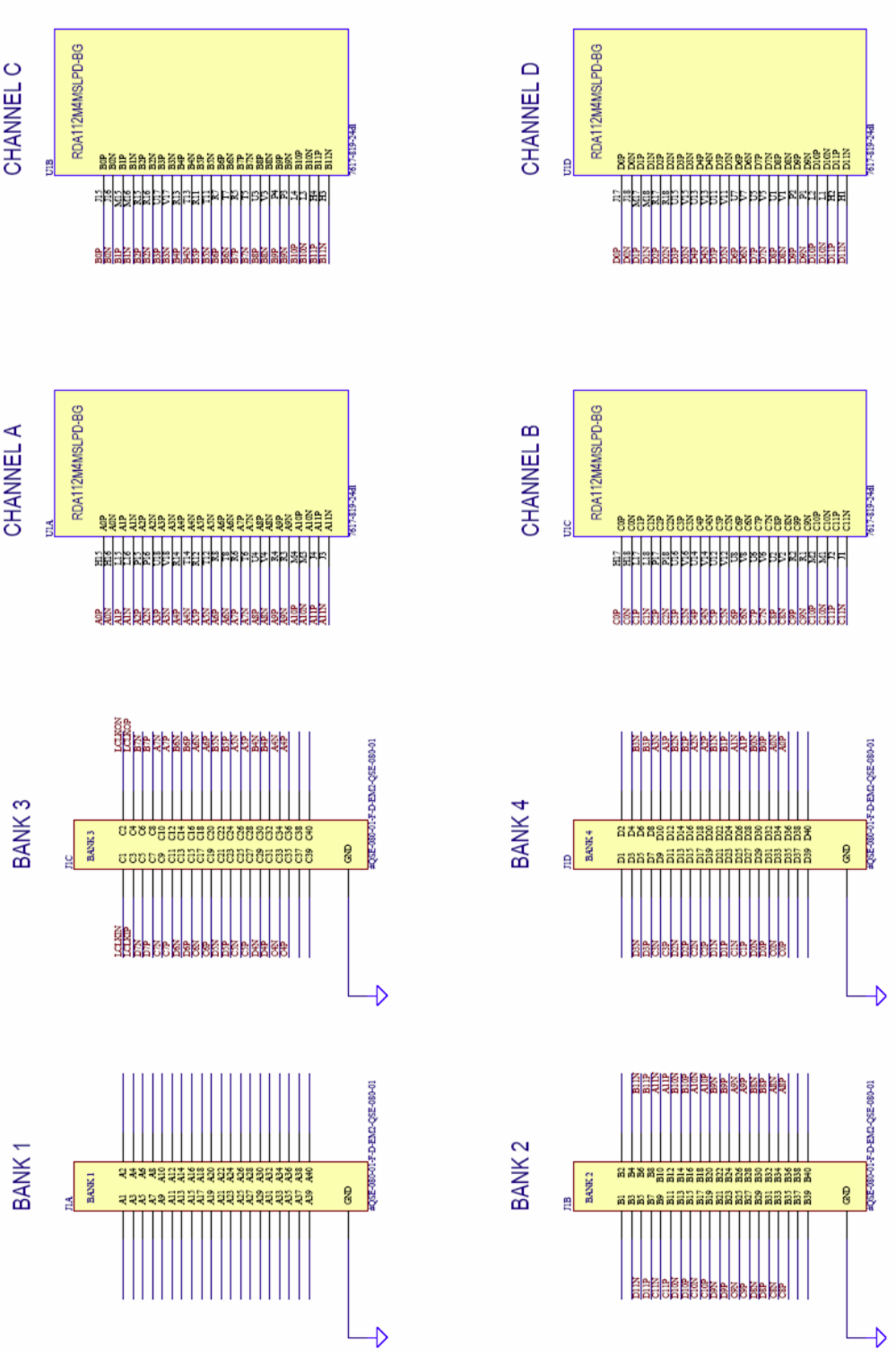

Figure 4-1 EVRDA112M4MSLPD Schematic Pg 1

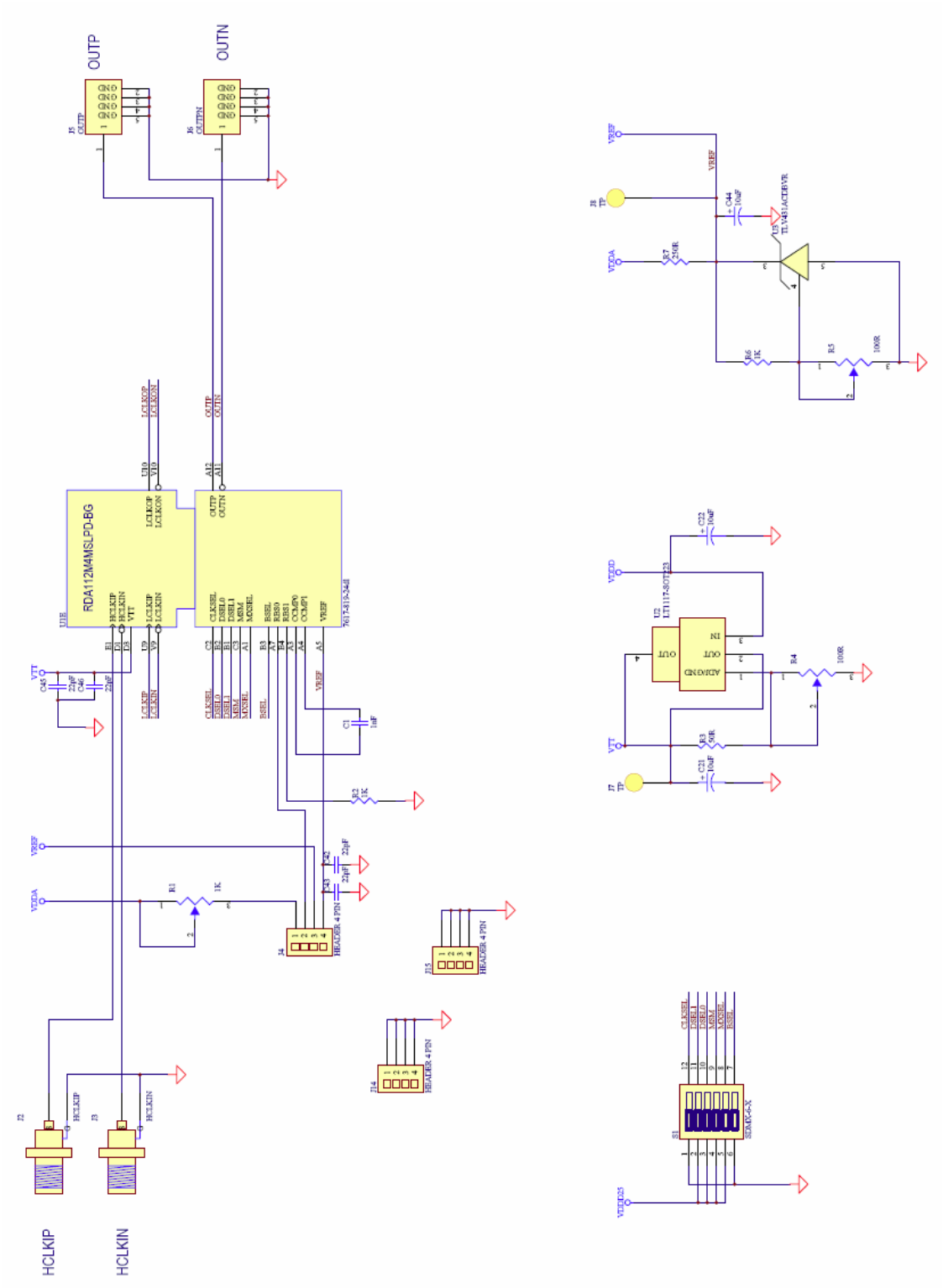

Figure 4-2 EVRDA112M4MSLPD Schematic Pg 2

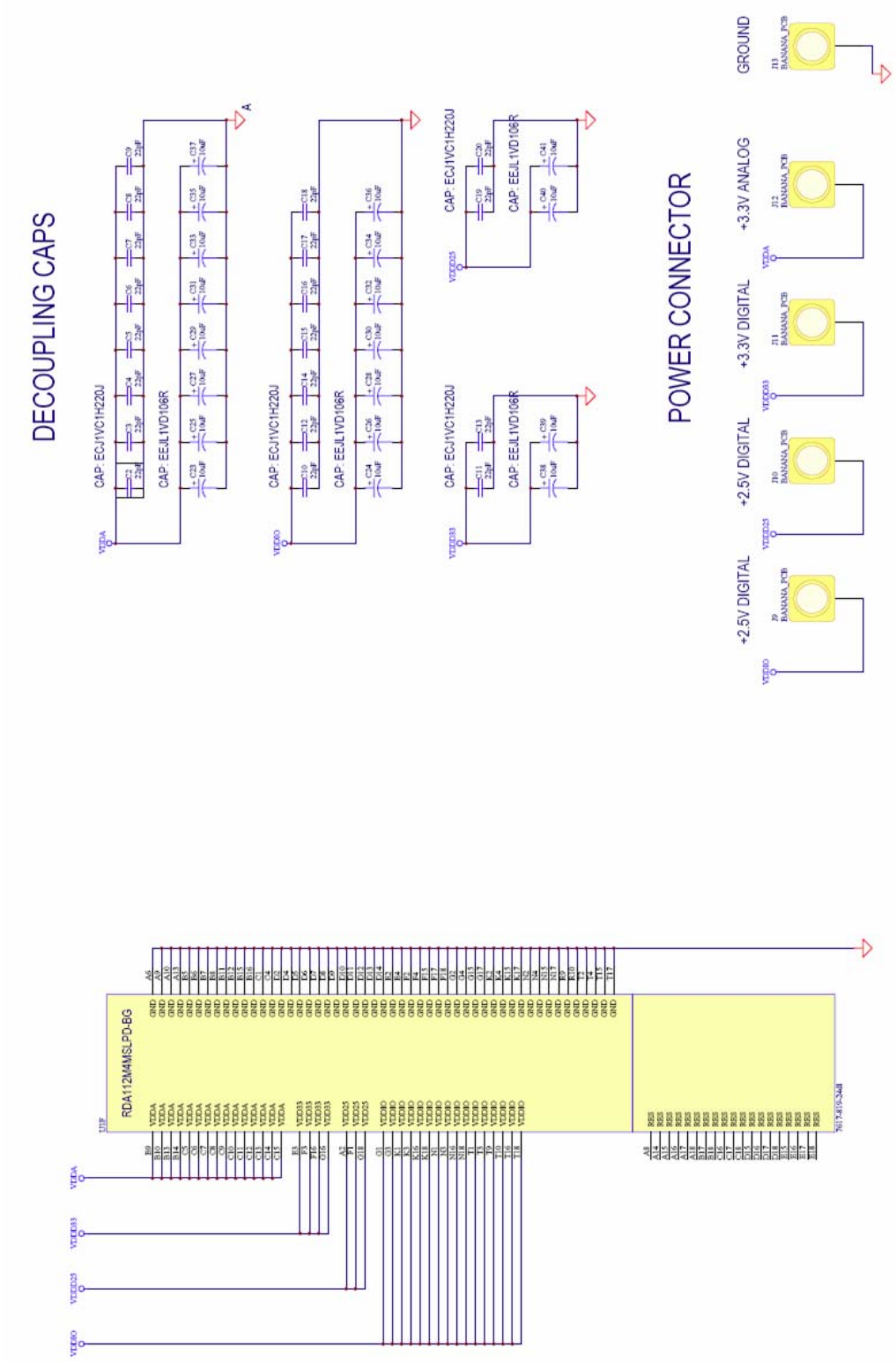

Figure 4-3 EVRDA112M4MSLPD Schematic Pg 3

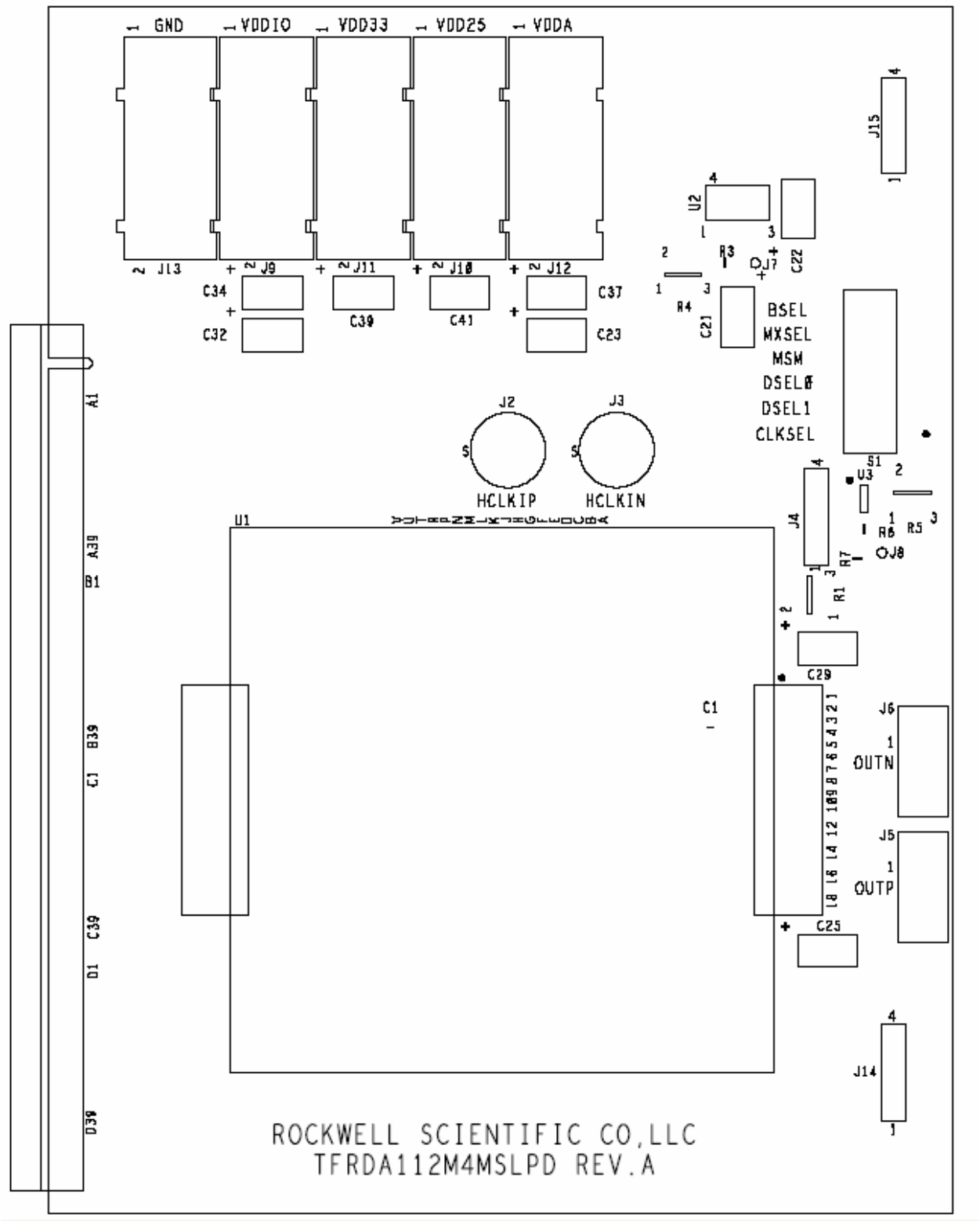

Figure 5 - Top layer stencil

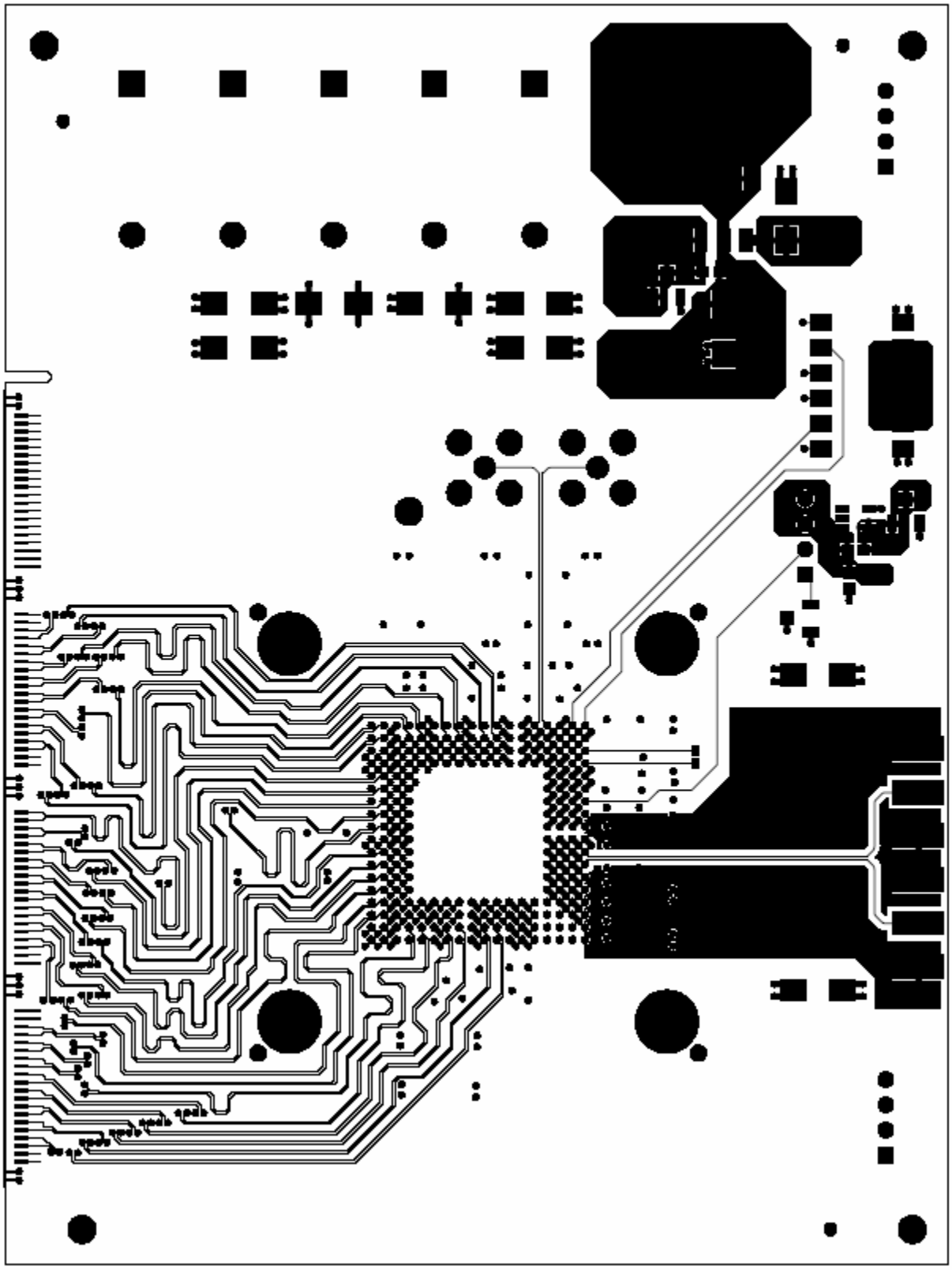

Figure 6 - Top layer

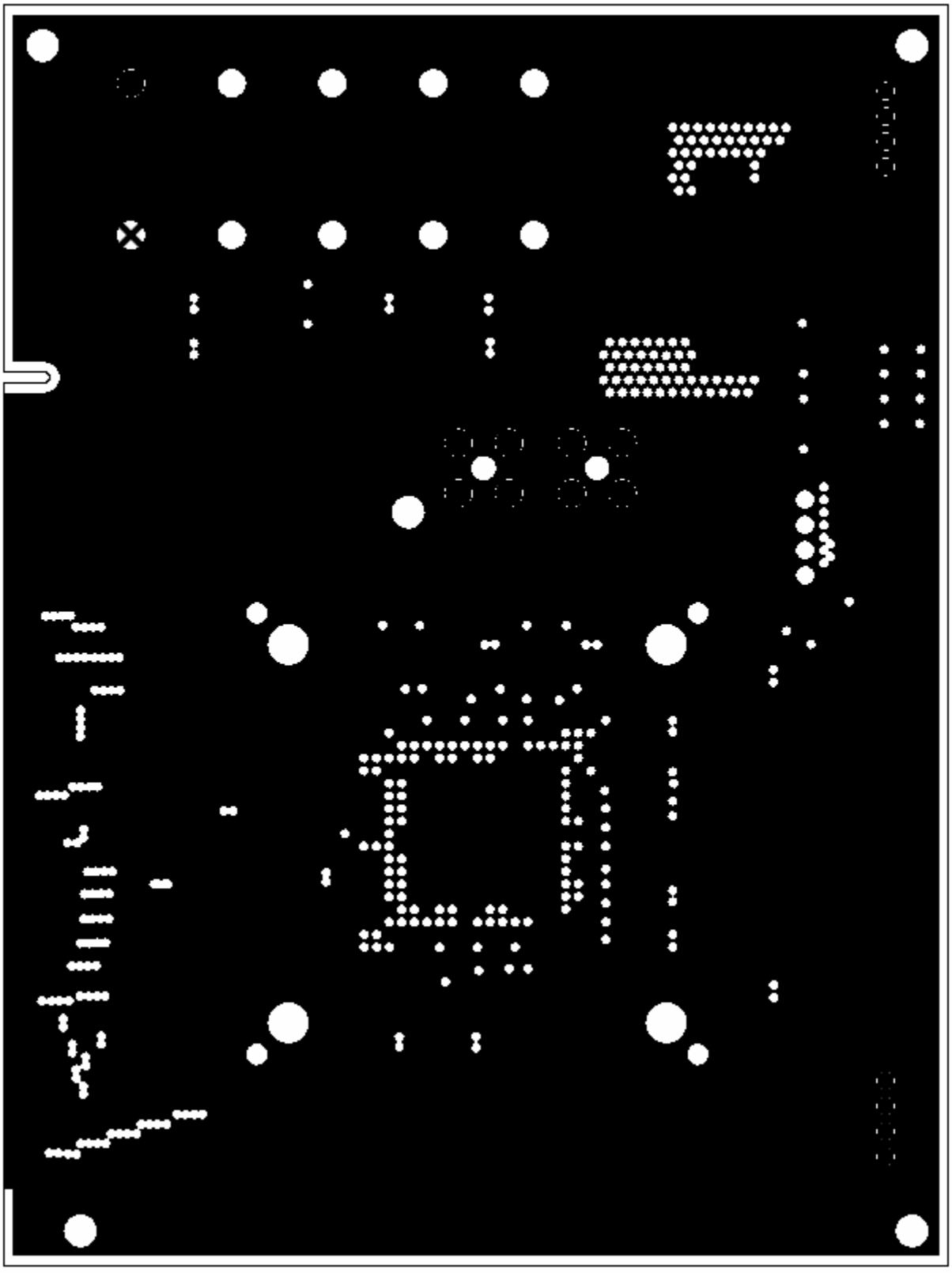

Figure 7 – GND (layer 2)

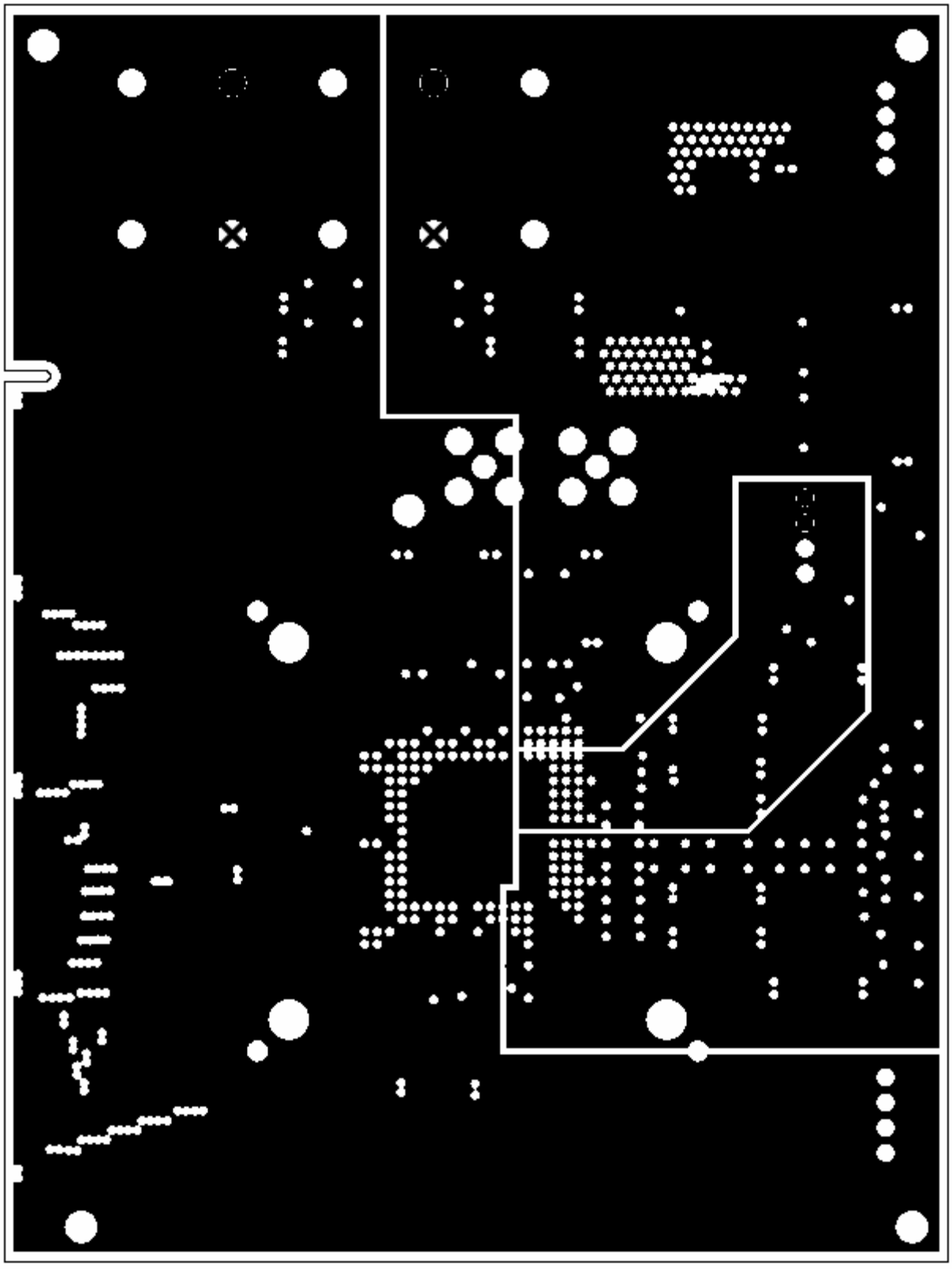

Figure 8 – Power Plane Layer 3

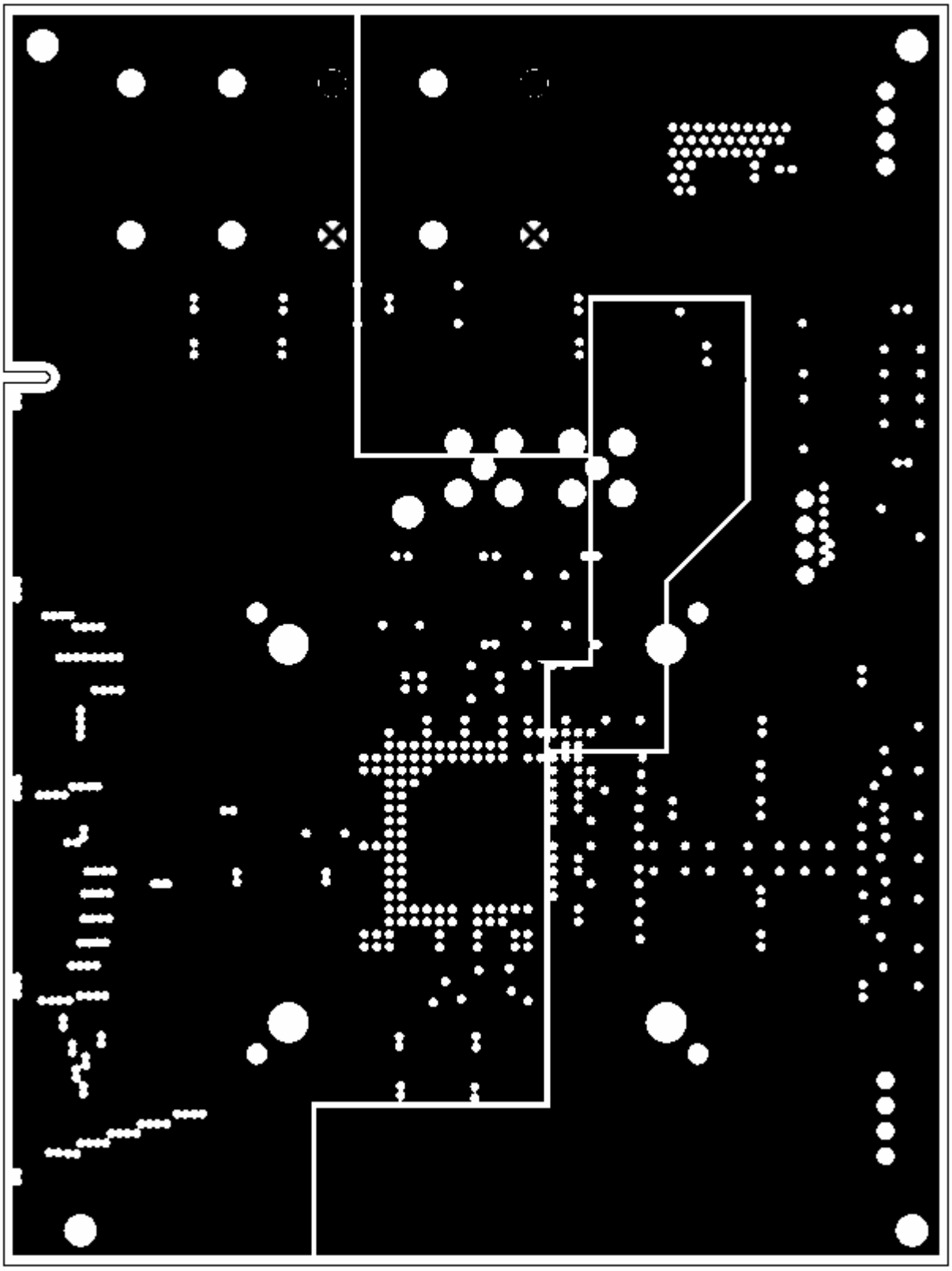

Figure 9 – Power Plane Layer 4

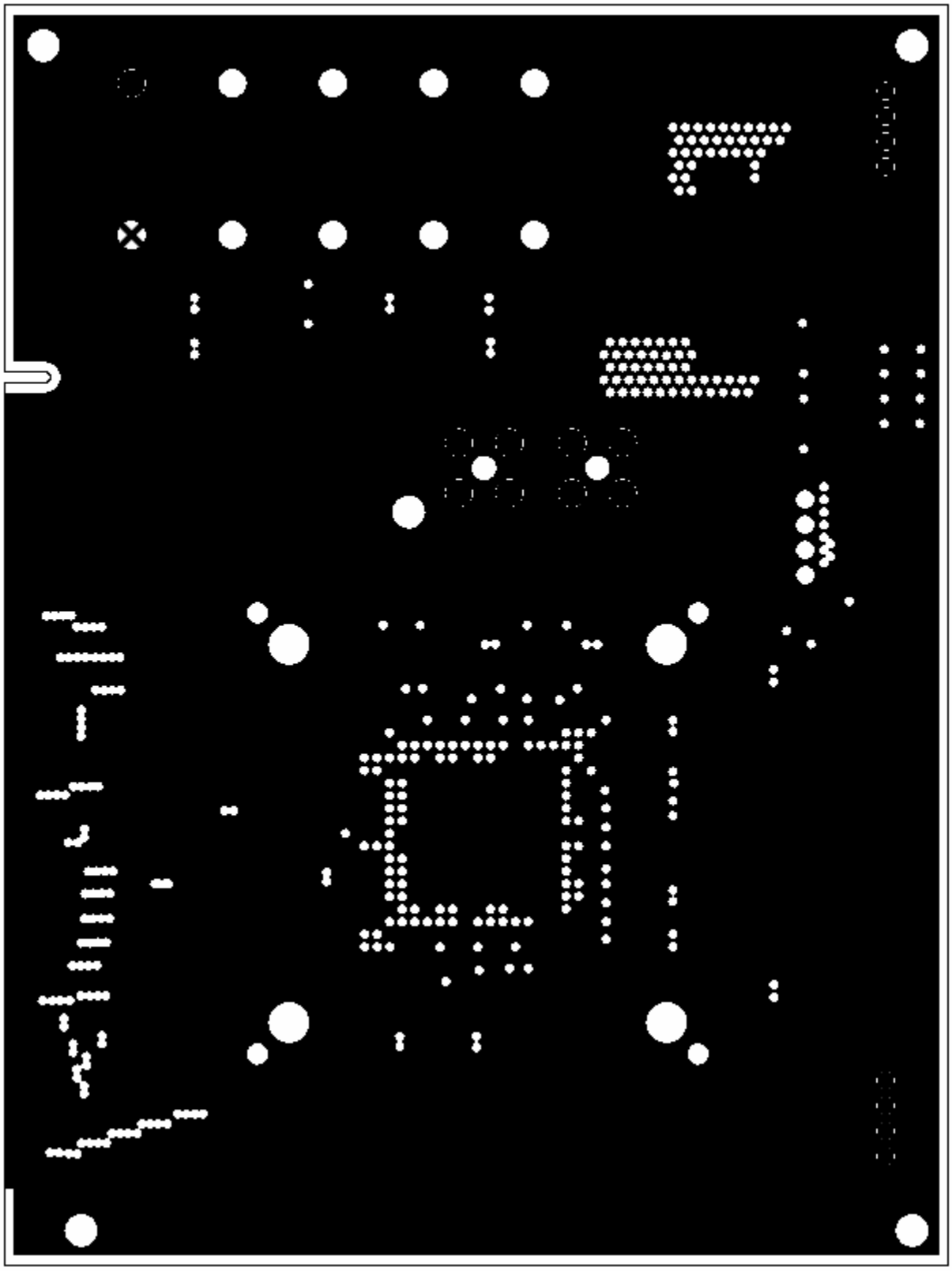

Figure 10 – Layer 5 (GND)

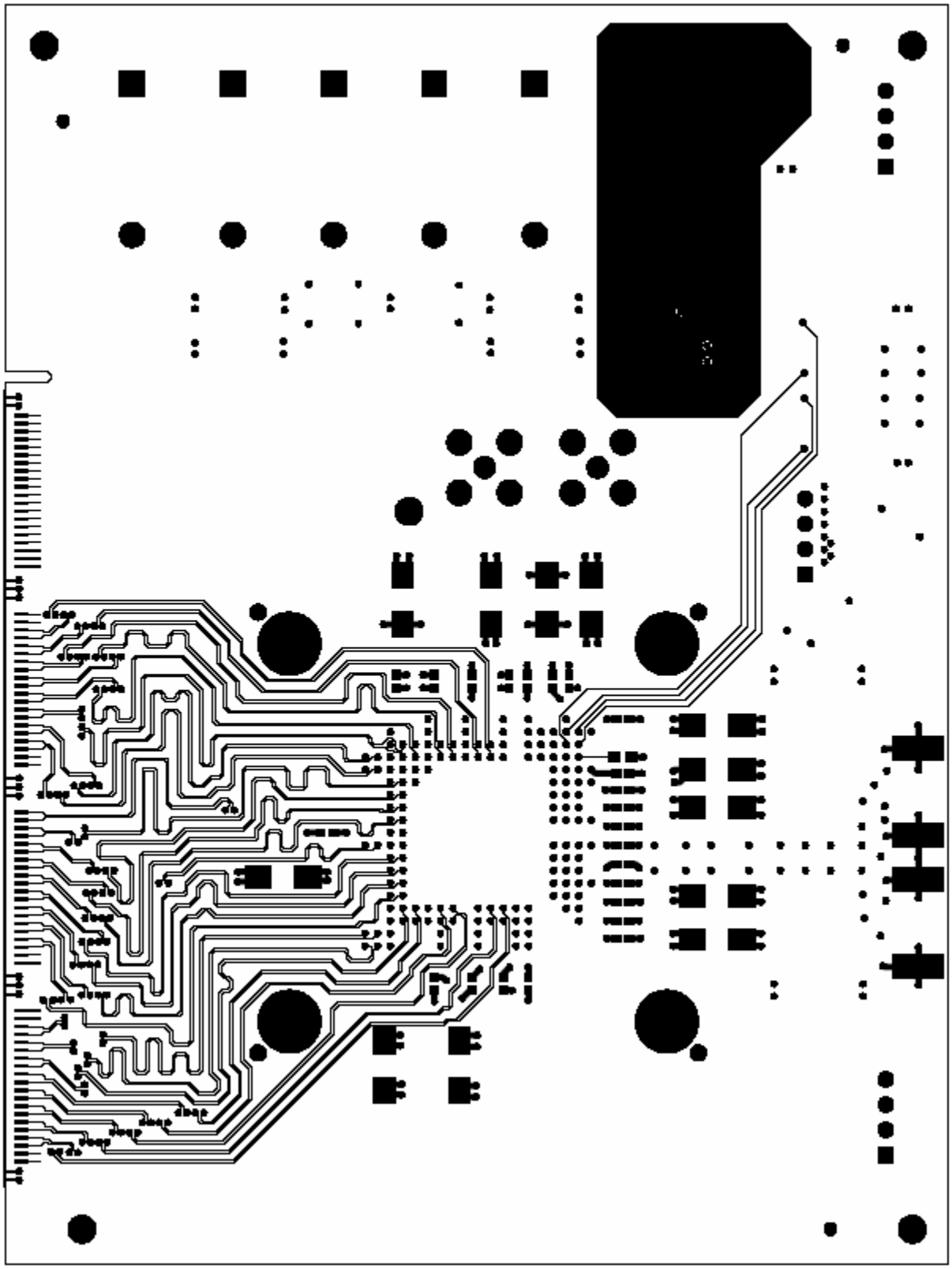

Figure 11 - Bottom layer

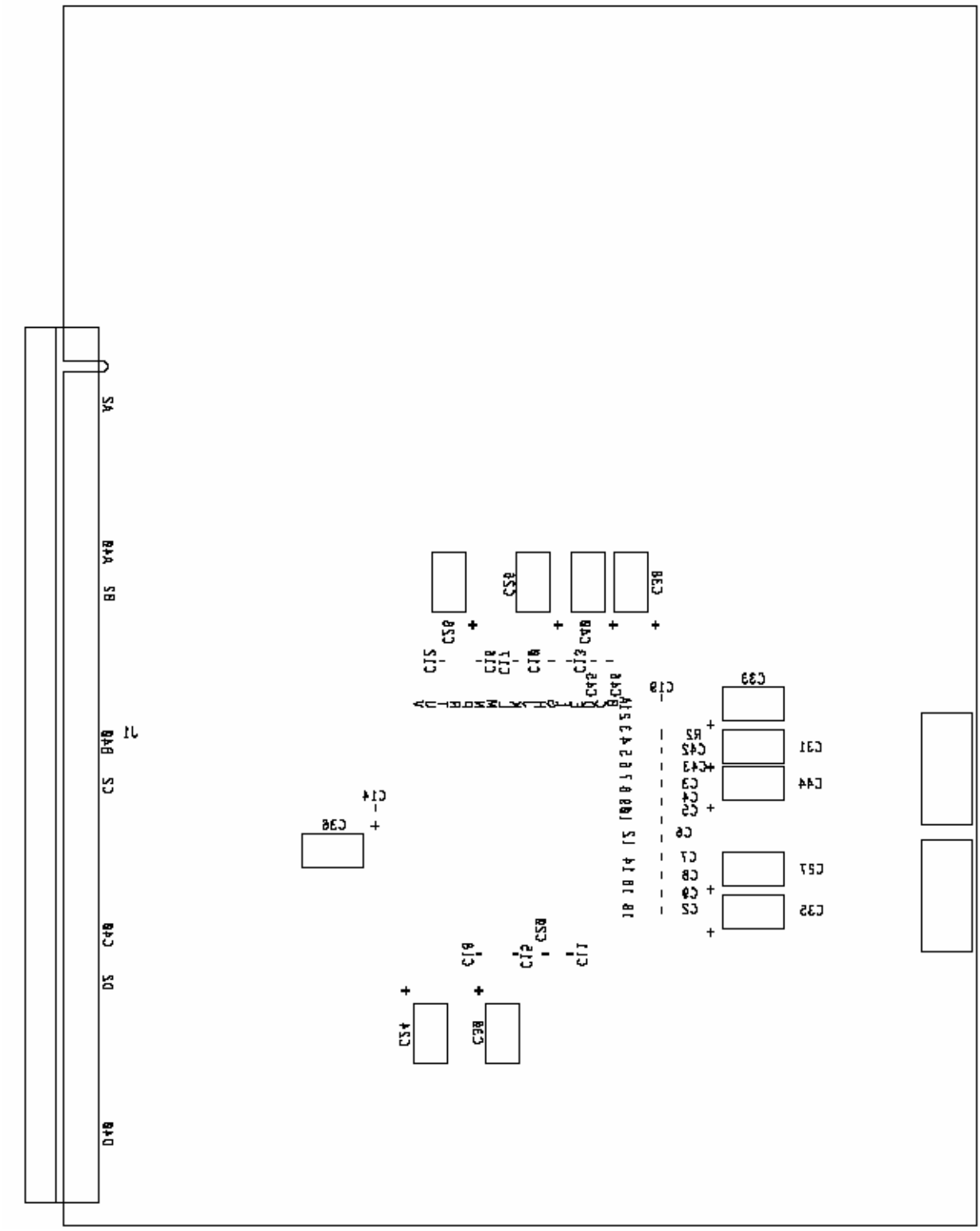

Figure 12 - Bottom layer stencil