TELEDYNE SCIENTIFIC COMPANY

EVRTH110

Track and Hold Evaluation Board

Features

- RF connectors for all signal / clock inputs and signal output.
- Fully Assembled and Tested.

Product Description

The EVRTH110 is an evaluation board designed to demonstrate the performance of the Teledyne Scientific RTH110-QN. The board comes fully assembled and tested, providing an easy way to evaluate the track and hold performance. All is needed are power, a differential input and clock signals.

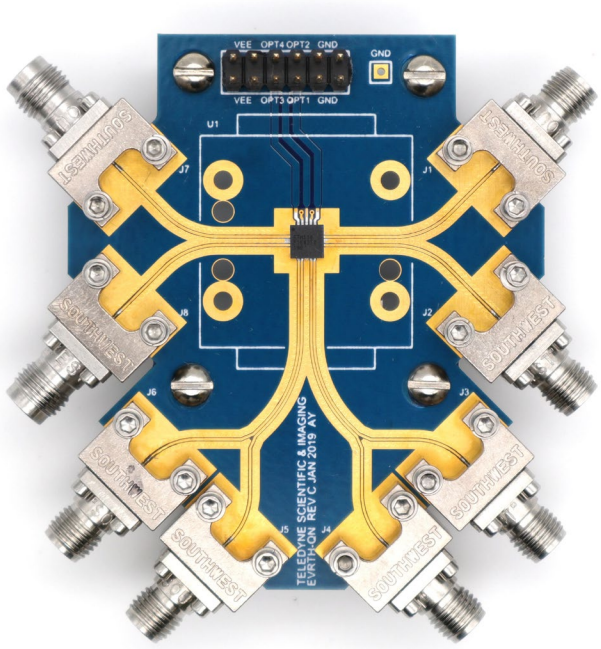

Figure 1– EVRTH110 Board

Ordering information

PART NUMBER	DESCRIPTION
EVRTH110	Track and Hold Evaluation Module with a RTH110-QN

Signal Description

P/I/O	PIN	NUM.	NAME	FUNCTION
P	1,2,3,4, 5	5	GND	Power Supply Ground
P	9,10,11,12	4	VEE	Negative Power Supply
I	SMA J5	1	CLKIP	Clock Input
I	SMA J6	1	CLKIN	
O	SMA J3	1	CLKOP	Clock Output
O	SMA J4	1	CLKON	
I	SMA J7	1	INP	Analog Input (2.4mm Connectors)
I	SMA J8	1	INN	
O	SMA J2	1	OUTP	Analog Output
O	SMA J1	1	OUTN	
I/O	6	1	TSEN	Temperature Sensor
I	8	1	CCAL	Current Cal: Connect to GND

Power Supplies

The evaluation board requires a negative supply voltage. VEE is a –5.2V supply (360mA nominal). The evaluation module also requires a ground connection. These connections are made using cables connected to the 6x2 pin power header located at the top of the board (Fig 4 and 5).

Inputs

The EVRTH110 evaluation board has high performance, 2.4mm connectors for the differential inputs. The clocks and outputs have SMA connectors. The signal inputs are terminated on-chip with 50Ω RF equivalent impedance to ground (refer to the RTH110 datasheet for the equivalent circuit).

It is recommended that the inputs are AC coupled. If a DC coupled connection is used the input common mode voltage should be observed (refer to the RTH110 datasheet). In case of a single ended connection, the unused input should be terminated with a 50Ω resistance to ground through a capacitor.

The clock CLKIP, CLKIN, is the clock for the three individual track and holds. It directly clocks the first track and hold. The clocks for the second and third track and holds are generated internally from CLKI. A copy of the internal generated clock is available at CLKOP, CLKON.

It is recommended that they are AC coupled, if not the clock signal should comply with the clock common mode voltage. When a single ended clock is used, the unused input should be terminated with a 50Ω resistance to ground through a capacitor.

The output clock CLKOP, CLKON can be used to drive the subsequent digitizing circuit such an ADC.

Outputs

The EVRTH110 has complementary outputs, OUTP and OUTN, accessible through high performance SMA connectors. Both outputs should be terminated with 50Ω impedance to ground (even if a single ended connection is used). For single ended applications an output balun may be used.

PCB Evaluation

Input Path Measurements

A PCB test board (Fig 2) was design with same geometry of the input path (replicated twice on the PCB). The attenuation was then measured using a PNA and the result is displayed in the graph below (Fig 3).

Figure 2– Input path test PCB.

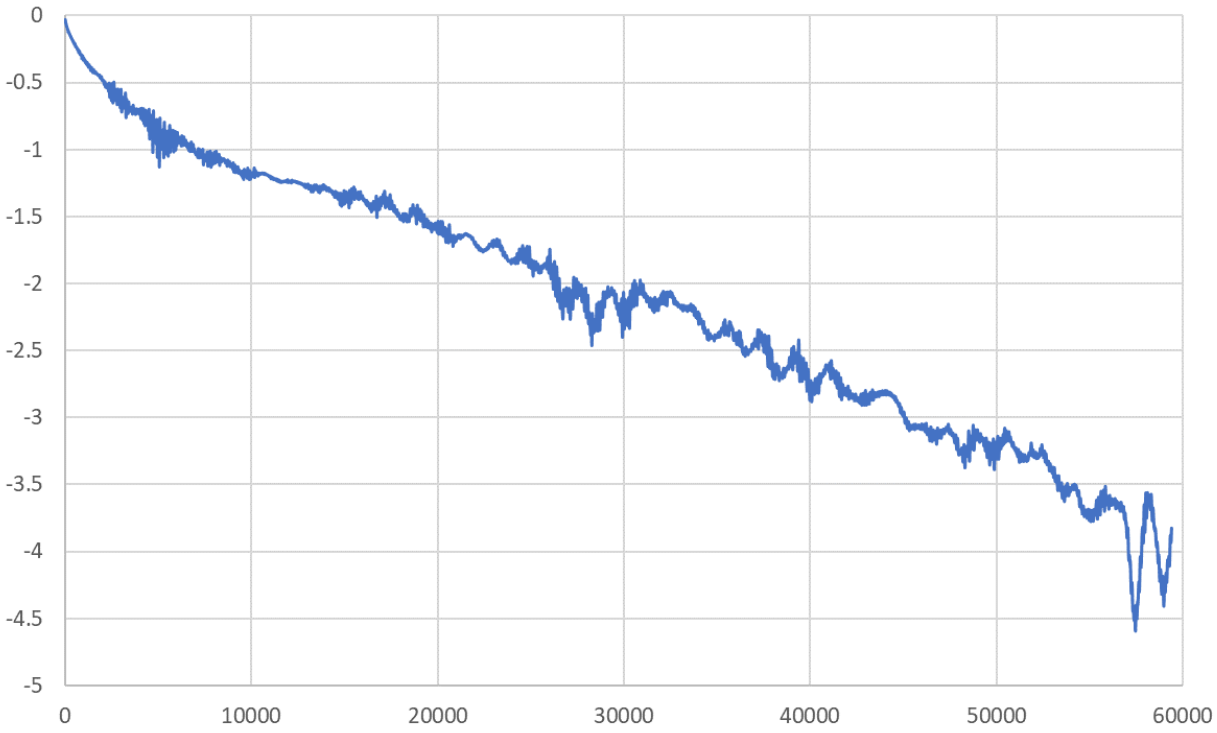

Figure 3– Input path attenuation.

Module Configuration

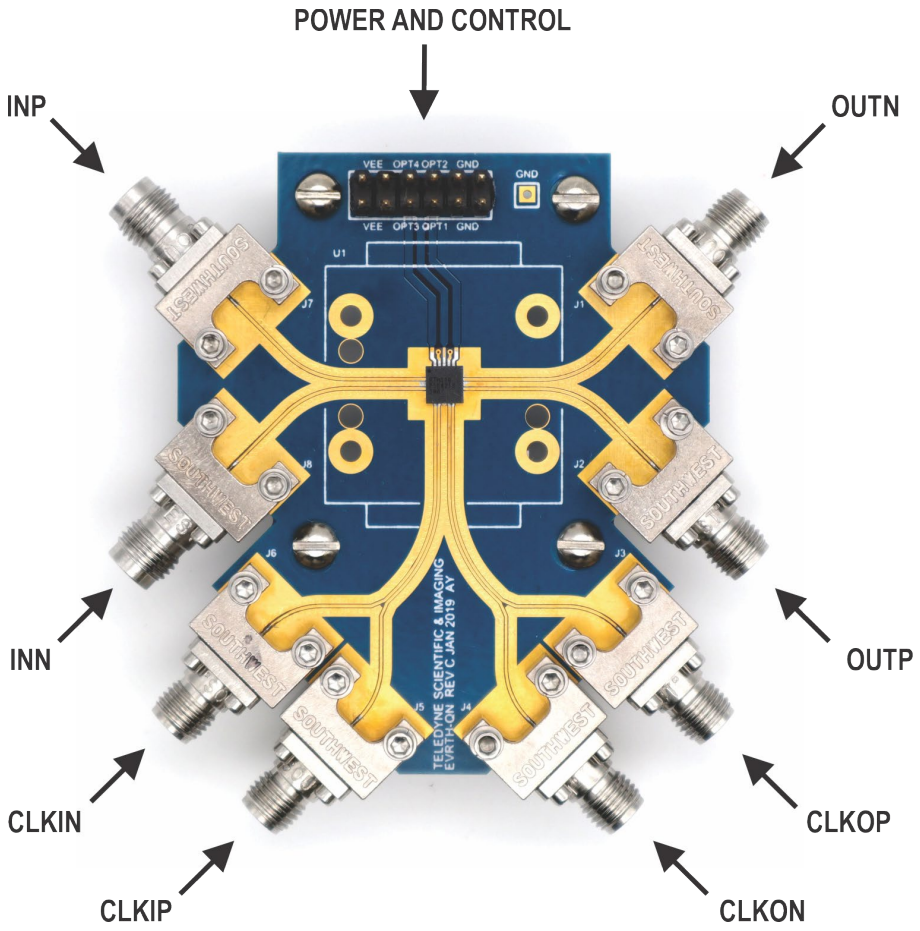

Figure 4 – Top view

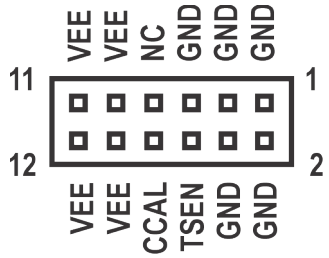

Figure 5 – Power and control connector