TELEDYNE
SCIENTIFIC COMPANY

RTH130

50 GHz Bandwidth High Sampling Rate

Track-and-Hold

REV-DATE PA0-1922
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DS

TELEDYNE SCIENTIFIC COMPANY

RTH130

50 GHz Bandwidth 14GS/s Track-and-Hold

Features

- 50 GHz Input Bandwidth
- Better than -35 dBc THD Over the Total Bandwidth with Small Signal Input
- Better than -35 dBc SFDR Over the Total Bandwidth with Small Signal Input
- 1 to 14 GHz Maximum Sampling Rate
- Differential Analog Input/Output
- Output Held more than Half Clock Cycle
- One Clock Operation
- 1.5W Power Dissipation
- Single Power Supply
- 4mm x 4mm QFN package

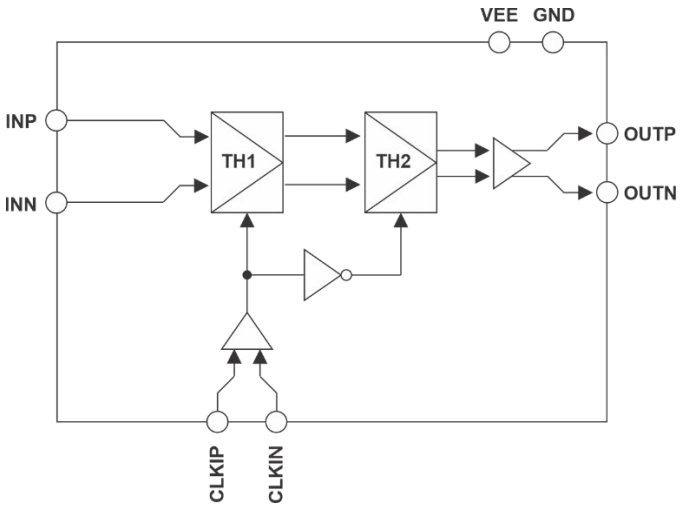

Figure 1 - Functional Block Diagram

Product Description

RTH130's bandwidth and aperture jitter enable 1 to 14 GS/s accurate sampling of DC to multi-GHz signals. The differential-to-differential dual track-and-hold cascades two track-and-hold circuits, TH1 and TH2. The RTH130 provides a held output for more than half a clock cycle, easing bandwidth requirements of subsequent circuitry relative to the case of a single track-and-hold (TH). The one clock operation further relaxes the timing requirements for sub-sampling applications.

Ordering information

PART NUMBER	DESCRIPTION
RTH130-QN	20 I/O QFN Package
RTH130-DI	Die
EVRTH130	Evaluation Board

CAUTION
DEVICE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)

Absolute Maximum Ratings

Supply Voltages

VEE to GND .....-5.5V

Input Voltages

INP, INN to GND .....-1V
CLKIP, CLKIN to GND ..... -1V

Temperature

Case Temperature .....+125°C
Junction Temperature ..... +150°C
Lead, Soldering (10 Seconds) ..... +220°C
Storage ..... -40 to 125°C

DC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.2V; Clock: 6000MHz, 0.6Vpp Differential; Input: 300mV Differential; Differential Outputs Terminated Into 50 Ω to 0V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
1.0	**DC TRANSFER FUNCTION**						
1.1	Gain	G			0		dB
2.0	**ANALOG INPUT (INP, INN)**						
2.1	Common Mode Voltage	IN_{CM}	Self Bias		0		mV
2.2	Input Impedance	R_{IIN}	Each Lead to GND		50		Ω
3.0	**CLOCK INPUT (CLKIP, CLKIN)**						
3.1	Input Resistance	R_{CIN}	Each Lead to GND		50		Ω
4.0	**ANALOG OUTPUT (OUTP, OUTN)**						
4.1	Output Resistance	R_{OUT}	Each Output to GND		50		Ω
4.2	Maximum Current		Into Output Lead			22	mA
4.3	Output Offset Voltage	V_{OFF}	Absolute Value (No Input Signal)		25		mV
4.4	Common Mode Voltage	OUT_{CM}	Outputs Terminated 50Ω to GND		-0.55		V
5.0	**POWER SUPPLY REQUIREMENTS**						
5.1	Negative Supply Current	IEE			290		mA
5.2	Power Dissipation	P			1.5		W

AC Electrical Specification – 6GHz Clock

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.2V; Clock: 6000MHz, 0.6Vpp Differential; Input: 300mV Differential; Differential Outputs Terminated Into 50 Ω to 0V.

6.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.3Vpp DIFFERENTIAL**						
6.1	Bandwidth	BW	-3dB Gain, 0.3 V_{PP} Differential Input	47	50		GHz
6.2	SFDR						
	2328 MHz	SFDR	0.3 Vpp Differential Input		52		dBc
	3078 MHz	SFDR	0.3 Vpp Differential Input		51		dBc
	3828 MHz	SFDR	0.3 Vpp Differential Input		60		dBc
	4578 MHz	SFDR	0.3 Vpp Differential Input		58		dBc
	5328 MHz	SFDR	0.3 Vpp Differential Input		59		dBc
	6078 MHz	SFDR	0.3 Vpp Differential Input		55		dBc
	6828 MHz	SFDR	0.3 Vpp Differential Input		58		dBc
	7578 MHz	SFDR	0.3 Vpp Differential Input		54		dBc
	8328 MHz	SFDR	0.3 Vpp Differential Input		50		dBc
	9078 MHz	SFDR	0.3 Vpp Differential Input		47		dBc
	9828 MHz	SFDR	0.3 Vpp Differential Input		51		dBc
	10578 MHz	SFDR	0.3 Vpp Differential Input		53		dBc
	11328 MHz	SFDR	0.3 Vpp Differential Input		52		dBc
	12078 MHz	SFDR	0.3 Vpp Differential Input		51		dBc
	12828 MHz	SFDR	0.3 Vpp Differential Input		53		dBc
	13578 MHz	SFDR	0.3 Vpp Differential Input		50		dBc
	14328 MHz	SFDR	0.3 Vpp Differential Input		48		dBc
	15078 MHz	SFDR	0.3 Vpp Differential Input		50		dBc
	15828 MHz	SFDR	0.3 Vpp Differential Input		56		dBc
	16578 MHz	SFDR	0.3 Vpp Differential Input		54		dBc
	17328 MHz	SFDR	0.3 Vpp Differential Input		55		dBc
	18078 MHz	SFDR	0.3 Vpp Differential Input		53		dBc
	18828 MHz	SFDR	0.3 Vpp Differential Input		54		dBc
	19578 MHz	SFDR	0.3 Vpp Differential Input		54		dBc
	20328 MHz	SFDR	0.3 Vpp Differential Input		46		dBc
	21078 MHz	SFDR	0.3 Vpp Differential Input		55		dBc
	21828 MHz	SFDR	0.3 Vpp Differential Input		54		dBc
	22578 MHz	SFDR	0.3 Vpp Differential Input		56		dBc
	23328 MHz	SFDR	0.3 Vpp Differential Input		52		dBc
	24078 MHz	SFDR	0.3 Vpp Differential Input		49		dBc
	24828 MHz	SFDR	0.3 Vpp Differential Input		52		dBc
	25578 MHz	SFDR	0.3 Vpp Differential Input		49		dBc
	26328 MHz	SFDR	0.3 Vpp Differential Input		46		dBc
	27078 MHz	SFDR	0.3 Vpp Differential Input		41		dBc
	27828 MHz	SFDR	0.3 Vpp Differential Input		48		dBc
	28578 MHz	SFDR	0.3 Vpp Differential Input		47		dBc
	29328 MHz	SFDR	0.3 Vpp Differential Input		45		dBc
	30078 MHz	SFDR	0.3 Vpp Differential Input		43		dBc
	30828 MHz	SFDR	0.3 Vpp Differential Input		46		dBc
	31578 MHz	SFDR	0.3 Vpp Differential Input		44		dBc
	32328 MHz	SFDR	0.3 Vpp Differential Input		43		dBc
	33078 MHz	SFDR	0.3 Vpp Differential Input		38		dBc
	33828 MHz	SFDR	0.3 Vpp Differential Input		46		dBc
	34578 MHz	SFDR	0.3 Vpp Differential Input		46		dBc
	35328 MHz	SFDR	0.3 Vpp Differential Input		45		dBc
	36078 MHz	SFDR	0.3 Vpp Differential Input		45		dBc
	36828 MHz	SFDR	0.3 Vpp Differential Input		46		dBc

6.2	SFDR						
	37578 MHz	SFDR	0.3 Vpp Differential Input		43		dBc
	38328 MHz	SFDR	0.3 Vpp Differential Input		39		dBc
	39078 MHz	SFDR	0.3 Vpp Differential Input		44		dBc
	39828 MHz	SFDR	0.3 Vpp Differential Input		37		dBc
	40578 MHz	SFDR	0.3 Vpp Differential Input		45		dBc
	41328 MHz	SFDR	0.3 Vpp Differential Input		44		dBc
	42078 MHz	SFDR	0.3 Vpp Differential Input		44		dBc
	42828 MHz	SFDR	0.3 Vpp Differential Input		44		dBc
	43578 MHz	SFDR	0.3 Vpp Differential Input		42		dBc
	44328 MHz	SFDR	0.3 Vpp Differential Input		39		dBc
	45078 MHz	SFDR	0.3 Vpp Differential Input		40		dBc
	45828 MHz	SFDR	0.3 Vpp Differential Input		40		dBc
	46578 MHz	SFDR	0.3 Vpp Differential Input		44		dBc
	47328 MHz	SFDR	0.3 Vpp Differential Input		43		dBc
	48078 MHz	SFDR	0.3 Vpp Differential Input		43		dBc
	48828 MHz	SFDR	0.3 Vpp Differential Input		48		dBc
	49578 MHz	SFDR	0.3 Vpp Differential Input		42		dBc
	50328 MHz	SFDR	0.3 Vpp Differential Input		41		dBc
	51078 MHz	SFDR	0.3 Vpp Differential Input		39		dBc
	51828 MHz	SFDR	0.3 Vpp Differential Input		45		dBc

AC Electrical Specification – 10GHz Clock

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.2V; Clock: 10000MHz, 0.6Vpp Differential; Input: 300mV Differential; Differential Outputs Terminated Into 50 Ω to 0V.

7.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.3Vpp DIFFERENTIAL**						
7.1	Bandwidth	BW	-3dB Gain, 0.3 V_{PP} Differential Input	47	50		GHz
	SFDR						
	2630 MHz	SFDR	0.3 Vpp Differential Input		57		dBc
	3880 MHz	SFDR	0.3 Vpp Differential Input		44		dBc
	5130 MHz	SFDR	0.3 Vpp Differential Input		44		dBc
	6380 MHz	SFDR	0.3 Vpp Differential Input		47		dBc
	7630 MHz	SFDR	0.3 Vpp Differential Input		56		dBc
	8880 MHz	SFDR	0.3 Vpp Differential Input		52		dBc
	10130 MHz	SFDR	0.3 Vpp Differential Input		52		dBc
	11380 MHz	SFDR	0.3 Vpp Differential Input		54		dBc
	12630 MHz	SFDR	0.3 Vpp Differential Input		47		dBc
	13880 MHz	SFDR	0.3 Vpp Differential Input		41		dBc
	15130 MHz	SFDR	0.3 Vpp Differential Input		42		dBc
	16380 MHz	SFDR	0.3 Vpp Differential Input		48		dBc
	17630 MHz	SFDR	0.3 Vpp Differential Input		55		dBc
	18880 MHz	SFDR	0.3 Vpp Differential Input		54		dBc
	20130 MHz	SFDR	0.3 Vpp Differential Input		52		dBc
	21380 MHz	SFDR	0.3 Vpp Differential Input		51		dBc
	22630 MHz	SFDR	0.3 Vpp Differential Input		52		dBc
	23880 MHz	SFDR	0.3 Vpp Differential Input		42		dBc
	25130 MHz	SFDR	0.3 Vpp Differential Input		43		dBc
7.2	26380 MHz	SFDR	0.3 Vpp Differential Input		44		dBc
	27630 MHz	SFDR	0.3 Vpp Differential Input		50		dBc
	28880 MHz	SFDR	0.3 Vpp Differential Input		44		dBc
	30130 MHz	SFDR	0.3 Vpp Differential Input		42		dBc
	31380 MHz	SFDR	0.3 Vpp Differential Input		43		dBc
	32630 MHz	SFDR	0.3 Vpp Differential Input		45		dBc
	33880 MHz	SFDR	0.3 Vpp Differential Input		41		dBc
	35130 MHz	SFDR	0.3 Vpp Differential Input		37		dBc
	36380 MHz	SFDR	0.3 Vpp Differential Input		42		dBc
	37630 MHz	SFDR	0.3 Vpp Differential Input		45		dBc
	38880 MHz	SFDR	0.3 Vpp Differential Input		45		dBc
	40130 MHz	SFDR	0.3 Vpp Differential Input		39		dBc
	41380 MHz	SFDR	0.3 Vpp Differential Input		44		dBc
	42630 MHz	SFDR	0.3 Vpp Differential Input		39		dBc
	43880 MHz	SFDR	0.3 Vpp Differential Input		37		dBc
	45130 MHz	SFDR	0.3 Vpp Differential Input		40		dBc
	46380 MHz	SFDR	0.3 Vpp Differential Input		41		dBc
	47630 MHz	SFDR	0.3 Vpp Differential Input		43		dBc
	48880 MHz	SFDR	0.3 Vpp Differential Input		46		dBc
	50130 MHz	SFDR	0.3 Vpp Differential Input		44		dBc
	51380 MHz	SFDR	0.3 Vpp Differential Input		45		dBc

AC Electrical Specification – 12GHz Clock

Test Conditions (see notes for specific conditions): Room Temperature; VEE = -5.2V; Clock: 12000MHz, 0.6Vpp Differential; Input: 300mV Differential; Differential Outputs Terminated Into 50 Ω to 0V.

8.0	**DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT, 0.3Vpp DIFFERENTIAL**						
8.1	Bandwidth	BW	-3dB Gain, 0.3 V_{PP} Differential Input	47	50		GHz
8.2	SFDR						
	3156 MHz	SFDR	0.3 Vpp Differential Input		48		dBc
	4656 MHz	SFDR	0.3 Vpp Differential Input		39		dBc
	6156 MHz	SFDR	0.3 Vpp Differential Input		38		dBc
	7656 MHz	SFDR	0.3 Vpp Differential Input		39		dBc
	9156 MHz	SFDR	0.3 Vpp Differential Input		53		dBc
	10656 MHz	SFDR	0.3 Vpp Differential Input		53		dBc
	12156 MHz	SFDR	0.3 Vpp Differential Input		50		dBc
	13656 MHz	SFDR	0.3 Vpp Differential Input		52		dBc
	15156 MHz	SFDR	0.3 Vpp Differential Input		47		dBc
	16656 MHz	SFDR	0.3 Vpp Differential Input		40		dBc
	18156 MHz	SFDR	0.3 Vpp Differential Input		41		dBc
	19656 MHz	SFDR	0.3 Vpp Differential Input		47		dBc
	21156 MHz	SFDR	0.3 Vpp Differential Input		54		dBc
	22656 MHz	SFDR	0.3 Vpp Differential Input		51		dBc
	24156 MHz	SFDR	0.3 Vpp Differential Input		49		dBc
	25656 MHz	SFDR	0.3 Vpp Differential Input		48		dBc
	27156 MHz	SFDR	0.3 Vpp Differential Input		46		dBc
	28656 MHz	SFDR	0.3 Vpp Differential Input		38		dBc
	30156 MHz	SFDR	0.3 Vpp Differential Input		37		dBc
	31656 MHz	SFDR	0.3 Vpp Differential Input		40		dBc
	33156 MHz	SFDR	0.3 Vpp Differential Input		45		dBc
	34656 MHz	SFDR	0.3 Vpp Differential Input		45		dBc
	36156 MHz	SFDR	0.3 Vpp Differential Input		45		dBc
	37656 MHz	SFDR	0.3 Vpp Differential Input		44		dBc
	39156 MHz	SFDR	0.3 Vpp Differential Input		40		dBc
	40656 MHz	SFDR	0.3 Vpp Differential Input		37		dBc
	42156 MHz	SFDR	0.3 Vpp Differential Input		37		dBc
	43656 MHz	SFDR	0.3 Vpp Differential Input		38		dBc
	45156 MHz	SFDR	0.3 Vpp Differential Input		39		dBc
	46656 MHz	SFDR	0.3 Vpp Differential Input		40		dBc
	48156 MHz	SFDR	0.3 Vpp Differential Input		39		dBc
	49656 MHz	SFDR	0.3 Vpp Differential Input		41		dBc
	51156 MHz	SFDR	0.3 Vpp Differential Input		42		dBc

Operating Conditions

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
11.0	**CLOCK INPUTS (CLKIP, CLKIN)**						
11.1	Amplitude	V_{CPP}	Differential		600		mVpp
11.2	Common Mode Voltage	V_{CCM}			0		mV
11.3	CLKI Frequency	F_{CLKI}		1		14	GHz
11.4	Rise and Fall Time	T_{RF}			50		ps
12.0	**ANALOG INPUT (INP, INN)**						
12.1	Full Scale Range	FSR	Differential			1000	mVpp
12.2	Common Mode Voltage	V_{CM}	When DC Coupled		0		mV
13.0	**ANALOG OUTPUT (OUTP, OUTN)**						
13.1	Ext. Termination Voltage	V_{TERM}				0.5	V
13.2	Ext. Termination Resistor	R_{TERM}	Required From Outputs To Vterm		50		Ω
14.0	**POWER SUPPLY REQUIREMENTS**						
14.1	Negative Supply Voltage	VEE		-5.0	-5.2	-5.4	V
15.0	**OPERATING TEMPERATURE**[1]						
15.1	Case Temperature	Tc		-40		85	°C

[1] The part is designed to maintain high performance operation within a case temperature range of -40 ~ 85°C and we recommend not to exceed the Absolute Maximum Temperature shown on page 2. For the best performance, operation within the specified temperature range with proper heat dissipation is recommended. The metal pad where the part is soldered should be connected to the ground plane with thermal vias for better heat dissipation. A heatsink can be attached to the bottom of the PCB, on a metal pad connected to the metal pad where the part is soldered.

Pin Description and Pin Out (20 I/O QFN Package)

P/I/O	PIN	NUM.	NAME	FUNCTION
P	1,3,5,8,9,10,11,13,15, bottom pad	9	GND	Power Supply Ground
P	17,18,19	3	VEE	Negative Power Supply
I	6	1	CLKIP	Clock Input: High = TH1 in Track Mode
I	7	1	CLKIN	Low = TH1 in Hold Mode
I	2	1	INP	Analog Input
I	4	1	INN	
O	14	1	OUTP	Analog Output
O	12	1	OUTN	
C	16	1	TSEN	Temperature Sensor
C	20	1	CCAL	Control: Connect to GND

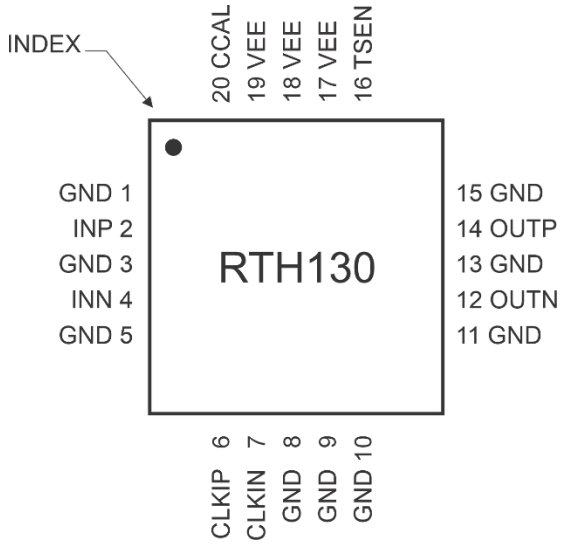

Figure 2 – RTH130 pinout (top view) 20 I/O QFN package.

Definitions of Terms

Acquisition Time (tacq). The delay between the time a track-and-hold circuit (TH) enters track mode and the time the TH hold capacitor nodes track the input within some specified precision. The acquisition time sets a lower limit on the required track time during clocked operation.

Aperture Delay (ta). The average (or mean value) of the delay between the hold command (input clock switched from track to hold state) and the instant at which the analog input is sampled. The time is positive if the clock path delay is longer than the signal path delay. It is negative if the signal path delay is longer than the clock path delay.

Aperture Jitter (Δt). The standard deviation of the delay between the hold command (input clock switched from track-to-hold state) and the instant at which the analog input is sampled, excluding clock source jitter. It is the total jitter if the clock source is jitter free (ideal). Jitter diverges slowly as measurement time increases because of "1/f" noise, important at low frequencies (< 10 kHz). The specified jitter takes into account the white noise sources only (thermal and shot noise). For high-speed samplers this is reasonable, since even long data records span a time shorter than the time scale important for 1/f noise. For white-noise caused jitter, the clock and aperture jitter can be added in an rms manner to obtain the total sampling jitter.

Clock Jitter. The standard deviation of the mid-points of the relevant (rising or falling) edge of the clock source relative to the ideal edge (best fit). This jitter can be derived from the phase noise of the clock source, where the lower frequency bound of integration should correspond to the duration of a measurement record that the source will be used for.

Common-Mode Rejection Ratio (CMRR). Proportionality coefficient of the differential output and the common mode component of input signal. If an ideal symmetric input is available, CMR is the ratio of the differential output to the input on either input pin. A high-quality 50-ohm splitter may be used to generate the symmetrical inputs.

Full Scale Range (FSR). The maximum difference between the highest and lowest input levels for which various device performance specifications hold, unless otherwise noted.

Gain. Ratio of output signal magnitude to input signal magnitude. For sinewave inputs, it is the ratio of the amplitude of the first (main) harmonic output (HD1) to the amplitude of the input.

Input Bandwidth (BW). The input frequency at which the gain for sinewave input is reduced by 3 dB relative to its value at low frequencies. The low frequency range is defined as the range including DC over which the gain stays essentially constant. The high frequency range is characterized by an increase in gain variation versus frequency, at least including the eventual monotonic decrease of the gain ("roll-off"). The input bandwidth tends to be input amplitude dependent. It is normally largest for very small inputs and smallest for FSR inputs.

Settling Time (ts). The delay between the time that a track-and-hold circuit (TH) enters hold mode and the time that the TH hold capacitor nodes settle to within some specified precision. The settling time sets a lower limit on the required hold time during clocked operation.

Spurious Free Dynamic Range (SFDR). The ratio of the magnitude of the first (main) harmonic, HD1, and the highest other harmonic (or non-harmonic other tone, if present), as observed in the TH spectrum. The input is FSR, unless otherwise noted. SFDR in dB is given by 20log (SFDR as amplitude ratio), and is generally positive.

Total Harmonic Distortion (THD). The ratio of the square root of the sum of the harmonics 2 to 5 to the amplitude of the first (main) harmonic in the TH spectrum. THD in dB is given by 20log (THD as amplitude ratio), and is generally negative.

Theory of Operation

The RTH130 contains two TH's, TH1, and TH2, in series, together with clock shaping circuitry, and a 50-ohm output driver. To maximize dynamic range and insensitivity to noise, all non-DC internal circuits and all non-DC inputs and outputs are differential. TH1 determines the dynamic sampled-mode performance of the Track and Hold. TH1 clock inputs, CLKIP and CLKIN, should be driven by a low-jitter clock source. TH2 get its clock from TH1 clock input.

The Track and Hold receives a differential analog input signal at inputs INP and INN, which is sampled on the TH1 hold capacitors upon a falling transition of its differential clock voltage V(CLKIP) – V(CLKIN), after an aperture delay, ta. The sampling instant is affected by clock source jitter (off-chip) and aperture jitter (caused by on-chip noise).

The held and buffered output of TH1, VTH1, is sampled on the TH2 hold capacitors after a fixed delay. TH2 clock have the opposite phase of the TH1 clock. Aperture jitter of TH2 is irrelevant, since TH1 will be in hold mode when TH2 capture the signal.

Since the clock for TH2 is generated internally only one clock source is need.

Signal Descriptions

The RTH130 inputs are terminated on-chip with equivalent 50Ω impedance to GND. This automatically protects against off-chip high-impedance high-voltage disturbances. The absolute maximum rated voltage at input termination resistors is -1 V. The RTH130 is designed for 1 Vpp differential input signals. If operated in single-ended mode, the complementary input needs to be terminated to ground with 50Ω. Distortion in the single-ended mode will be higher than in differential mode, and differential input should be used for optimal performance. The INP and INN inputs are equivalent, except for the polarity of their effect on OUTP and OUTN.

Both clock input signals are terminated on-chip with 50Ω to GND. Use differential clock signals for optimal performance. Large CLKI edge rate benefits aperture jitter performance, small CLKI amplitudes minimizes distortion due to clock feed-through in the higher clock frequency range. The RTH130 can also operate using single ended clocks (the unused input should be terminated). Distortion for single-ended clocks can be several dB higher than for differential clocks, and differential clocks should be used for optimal performance.

Due to its highly differential design, the RTH130 requires relatively modest power supply decoupling. The smaller decoupling capacitors from VEE to GND should be placed as close to the package as possible. Larger low frequency power supply decoupling capacitors, VEE to GND, should be placed within 1 inch of the RTH130. Depending on the expected noise on the supplies more capacitors in parallel may need to be used. With low-impedance supplies that are very quiet (no digital circuitry), the RTH130 can also perform well with no external decoupling at all.

Typical Operating Circuit

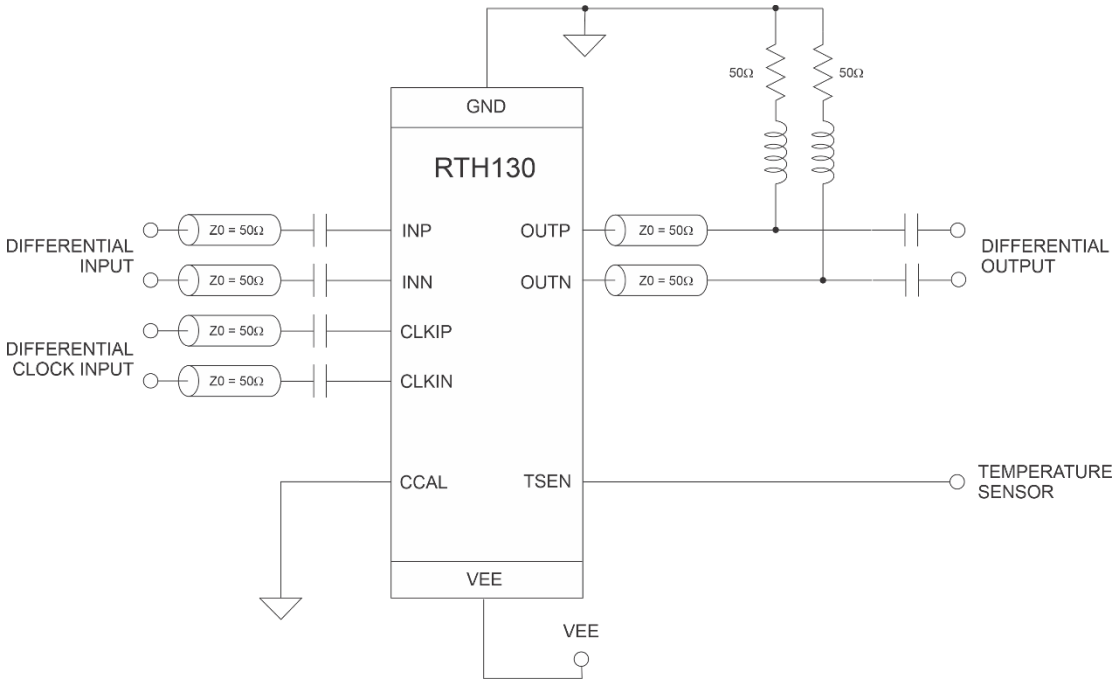

Figure 3 - Typical operating circuit.

Equivalent Circuit

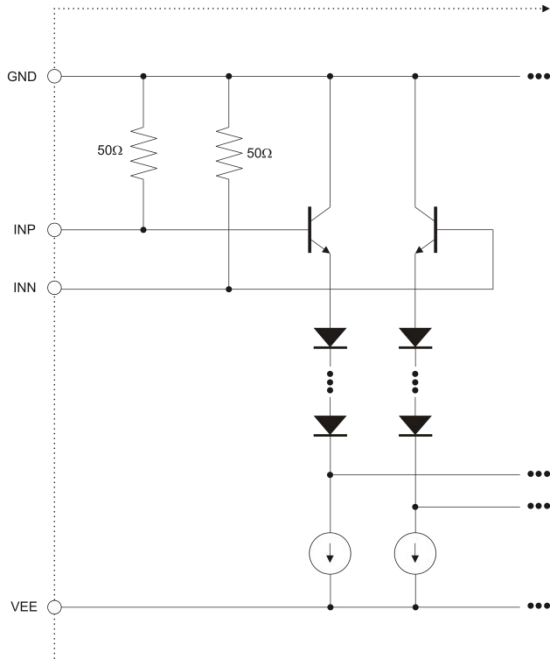

Figure 4 - Input circuit.

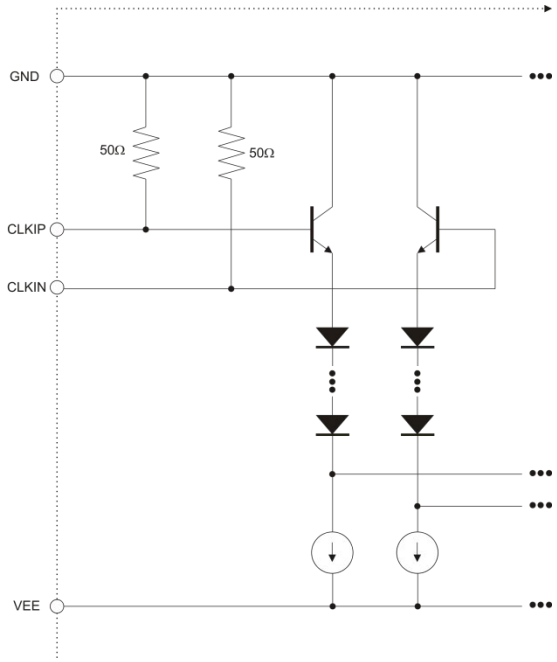

Figure 5 - Clock Input circuit.

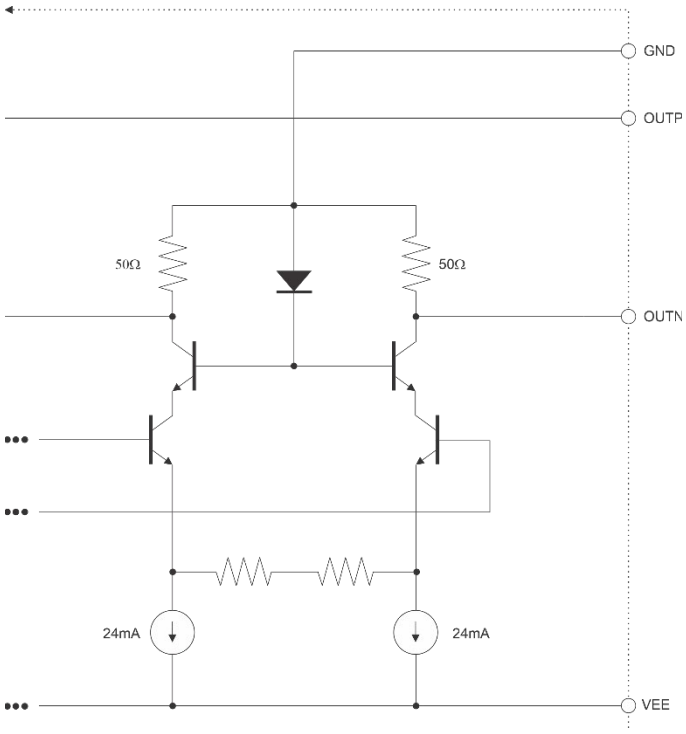

Figure 6 - Output circuit.

Typical Performance, Differential Input

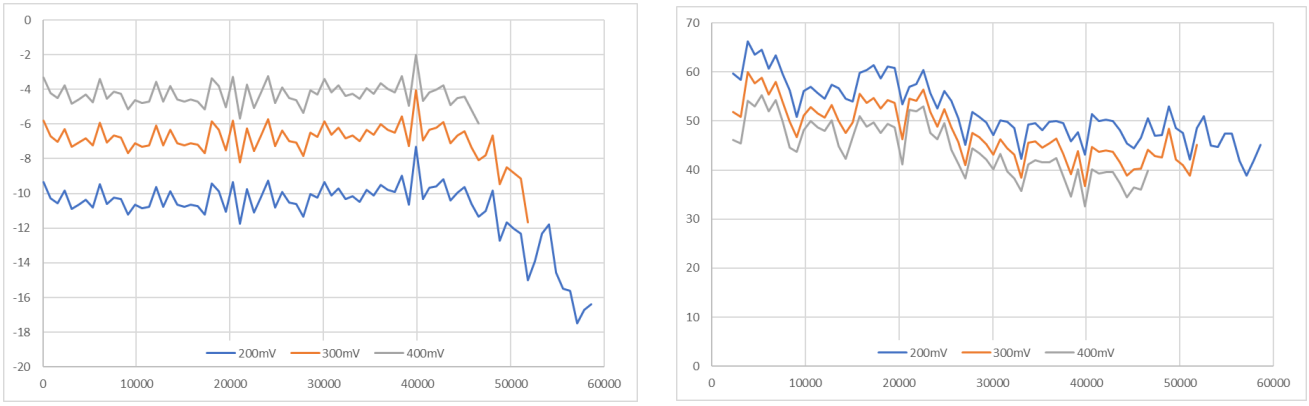

Figure 7 - Input Bandwidth (left) and SFDR (right) for 6GHz clock.

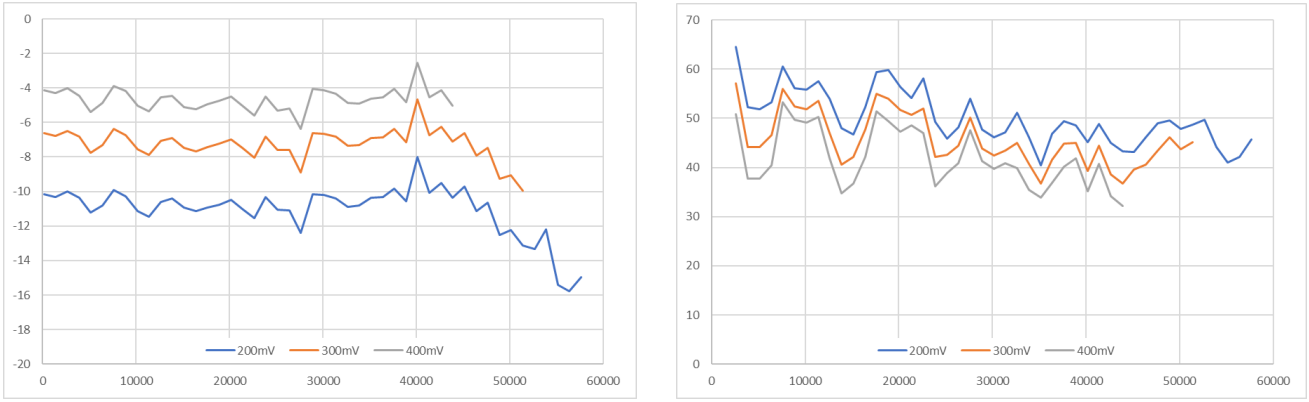

Figure 8 - Input Bandwidth (left) and SFDR (right) for 10GHz clock.

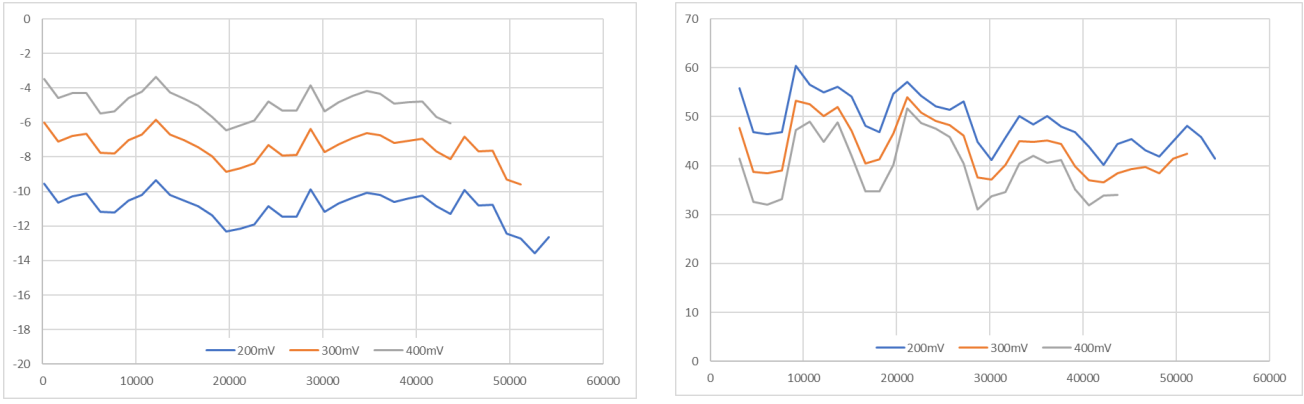

Figure 9 - Input Bandwidth (left) and SFDR (right) for 12GHz clock.

Package Information -QN

The package is an organic laminate 20 IO QFN.

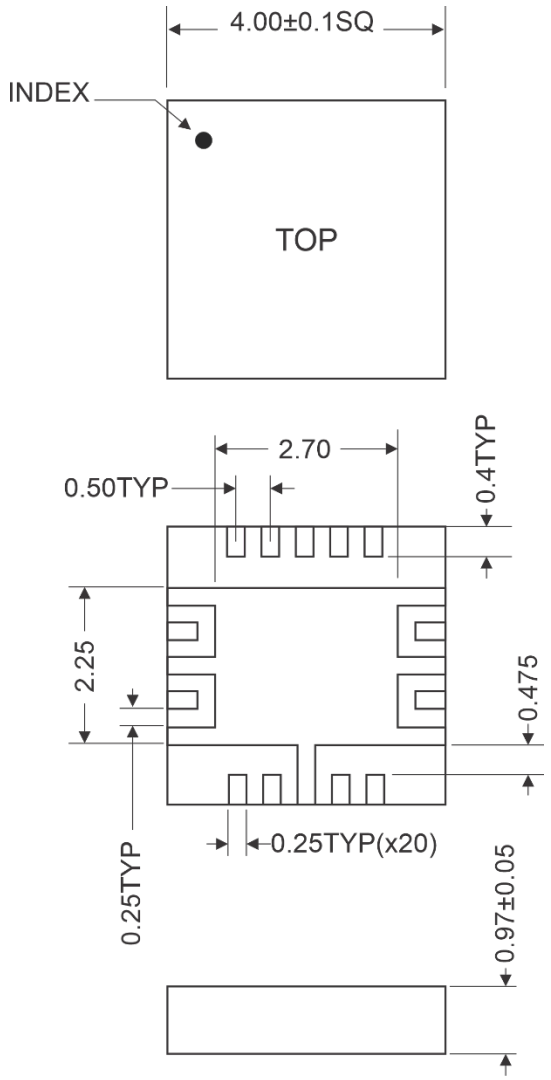

Figure 10 – RTH130-QN package outline, dimensions in mm.